FORCE COMPUTERS
A SOLECTRON COMPANY

SPARC/CPU-56

Reference Guide

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Headquarters

The Americas

Force Computers Inc.
4211 Starboard Drive
Fremont CA 94538

Tel.: +1 (510) 624-5300
Fax: +1 (510) 624-5301
Email: support@fci.com

Europe

Force Computers GmbH
Lilienthalstr. 15
D-85579 Neubiberg/München

Tel.: +49 (89) 608 14-0
Fax: +49 (89) 609 77 93
Email: support-de@fci.com

Asia

Force Computers Japan K.K.
Shibadaimon MF Bldg. 4F
Shiba Daimon 2-1-16
Minato-ku, Tokyo 105-0012
Tel.: +81 (03) 3437 3948
Fax: +81 (03) 3437 3968
Email: support-de@fci.com

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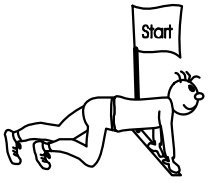
Using this Guide

This Reference Guide is intended for users qualified in electronics or electrical engineering. Users must have a working understanding of Peripheral Component Interconnect (PCI), VMEbus, and telecommunications.

Conventions

Notation	Description
57	All numbers are decimal numbers except when used with the notations described below.
00000000_{16}	Typical notation for hexadecimal numbers (digits 0 through F), e.g. used for addresses and offsets
0000_2	Same for binary numbers (digits 0 and 1)
x	Generic use of a letter
n	Generic use of numbers
n.nn	Decimal number
Bold	Used to emphasize a word
`Courier`	Used for on–screen output
`Courier+Bold`	Used to characterize user input
Italics	For references, table, and figure descriptions
File > *Exi*t	Notation for selecting a submenu
<text>	Notation for variables and keys
[text]	Notation for buttons
...	Repeated item
. . .	Omission of information from example/command that is not necessary at the time being
..	Ranges
:	Extents
|	Logical OR
——————— Note: ———————	No danger encountered. Pay attention to important information

Notation	Description
	Possibly dangerous situation: slight injuries to people or damage to objects possible
	Dangerous situation: injuries to people or severe damage to objects possible
	Start of a procedure
	End of a procedure

Abbreviations

Abbreviation	Description
B	
BGA	Ball Grid Array
BIB	Board Information Block
BMC	Base Board Management Controller
C	
CAS	Column Address Select
CSR	Control Status Register
D	
DMA	Direct Memory Access
DRAM	Dynamic Random Access Memory
E	
ECC	Error–Correction Code
EEPROM	Electrically Erasable Programmable Read–Only Memory
EPROM	Erasable Programmable Read Only Memory
ESD	Electrostatic Sensitive Device

Abbreviation	Description
F	
FAE	Field Application Engineers
FIFO	First In First Out
FPGA	Field-Programmable Gate Array
I	
IBMU	Intelligent Board Management Unit
ICMB	Intelligent Chassis Management Bus
ICT	In-Circuit Test
IDE	Integrated Drive Electronics
IEC	International Electric Code
IOBP	Input Output Back Panel
IOM	I/O Memory Management Unit
IPMB	Intelligent Platform Management Bus
IPMI	Intelligent Platform Management Interface
ISO	International Organization for Standardization
J	
JTAG	Joint Test Access Group
L	
LCA	Load Controller Assembly
LDO	Local Data Output
LED	Light Emitting Diode
LVD	Low Voltage Differential
LVTTL	Low Voltage Transistor Transistor Logic
M	
MAC	Media Access Control Layer
MCU	Memory Control Unit
MII	Media Independent Interface
N	
NEBS	Network Equipment Building Standards
NMI	Nonmaskable Interrupt
NVRAM	Nonvolatile Random Access Memory
O	
OBDIAG	OpenBoot Diagnostics
P	
PBM	PCI Bus Module
PCB	Printed Circuit Board
PCI	Peripheral Component Interconnect
PCIO	Peripheral Component Interconnect Input/Output
PHY	Physical Layer

Abbreviation	Description
PIE	PCI Interrupt Engine
PLCC	Plastic Leadless Chip Carrier
PLL	Phase-Locked Loop
PMC	PCI Mezzanine Card
POST	Power-On Self-Test
PROM	Programmable Read Only Memory
R	
RIC	Reset/Interrupt/Clock Controller
ROM	Read Only Memory
RTB	Rear Transition Board
RTC	Real-Time Clock
RTOS	Real Time Operating System
S	
SDRAM	Synchronous DRAM
SELV	Safety Extra Low Voltages
SPD	Serial Presence Detect
SRAM	Static Random Access Memory
STP	Shielded Twisted Pair
T	
TPE	Twisted Pair Ethernet
U	
UART	Universal Asynchronous Receiver-Transmitter
UIC	UPA Interrupt Connector
USB	Universal Serial Bus
UTP	Unshielded Twisted Pair
V	
VME	Versa Module Eurocard

Revision History

Order No.	Rev.	Date	Description
220225	AA	May 2003	Preliminary Manual
220225	AB	September 2003	Final release version
223147	AA	April 2004	Corrected number of SUN patch for audio support. Now it reads 109896–17. Updated order numbers in section ″Ordering Information″; added note to abort/reset key description; corrected feature list of FRctrl Solaris driver

Other Sources of Information

For further information refer to:

Company	www.	Document
ALI Corporation	ali.com.tw	ALI M1535D+ Southbridge documentation
Force Computers	forcecomputers.com	SPARC/IOBP-CPU-56 Installation Guide
		SPARC/MEM-550 Installation Guide
		ACC/CABLE/SCSI-U160 Installation Guide
		ACC/CABLE/RS422 Installation Guide
IEEE Standards Department	ieee.com	IEEE P1386 Standard Mechanics for a Common Mezzanine Card Family: CMC
Intel	intel.com	Intel 82540 Ethernet controller specifications
		Intel LXT971 PHY device specifications
LSI Logic	lsilogic.com	53C1010 SCSI controller specifications
Maxim	maxim-ic.com	MAX1617 temperature sensor specifications
STMicroelectronics	st.com	M48T35AV RTC/NVRAM specifications
National Semiconductor	national.com	PC87307/PC97307 Plug and Play Compatible Super I/O, Preliminary Specification, March 1998
PCI Special Interest Group	pcisig.com	PCI Local Bus Specification Rev2.1
PICMGPCI Special Interest Group	picmg.org pcisig.com	PCI Local Bus Specification Rev2.2
SUN	sun.com	UltraSPARCIIi+ Processor specifications
		SUN SME2300 PCIO-2 controller documentation
Tundra	tundra.com	Universe II documentation
VITA	vita.com	VME64 Standard ANSI/VITA 1-1994

Company	www.	Document
		VME64 Extensions Draft Standard, Draft 1.8, Jun 13, 1997
Xilinx	xilinx.com	Spartan XC520XL FPGA specifications

Safety Notes

The text in this chapter is a translation of the “Sicherheitshinweise” chapter

This section provides safety precautions to follow when installing, operating, and maintaining the board.

We intend to provide all necessary information to install and handle the board in this Installation Guide. However, as the product is complex and its usage manifold, we do not guarantee that the given information is complete. If you need additional information, ask your Force Computers representative.

The board has been designed to meet the standard industrial safety requirements. It must not be used except in its specific area of office telecommunication industry and industrial control.

Only personnel trained by Force Computers or persons qualified in electronics or electrical engineering are authorized to install, remove or maintain the board. The information given in this manual is meant to complete the knowledge of a specialist and must not be taken as replacement for qualified personnel.

EMC

The board has been tested in a Standard Force Computers system and found to comply with the limits for a Class A digital device in this system, pursuant to part 15 of the FCC Rules respectively EN 55022 Class A. These limits are designed to provide reasonable protection against harmful interference when the system is operated in a commercial environment.

The board generates and uses radio frequency energy and, if not installed properly and used in accordance with this Installation Guide, may cause harmful interference to radio communications. Operating the system in a residential area is likely to cause harmful interference, in which case the user will be required to correct the interference at his own expense.

To ensure proper EMC shielding, always operate the board with the blind panel or with PMC module installed. If boards are integrated into open systems, always cover empty slots.

Switch Settings

Switches marked as ’reserved’ might carry production–related functions and can cause the board to malfunction if their setting is

changed. Therefore, only change settings of switches not marked as 'reserved'.

Setting/resetting the switches during operation causes board damage. Therefore, check and change switch settings before you install the board.

Installation

Electrostatic discharge and incorrect board installation and removal can damage circuits or shorten their life. Therefore:

- **Touching the board or electronic components in a non–ESD protected environment causes component and board damage. Before touching boards or electronic components, make sure that you are working in an ESD–safe environment.**
- **When plugging the board in or removing it, do not press or pull on the front panel but use the handles.**
- **Before installing or removing an additional device or module, read the respective documentation.**
- **Make sure that the board is connected to the VME backplane via all assembled connectors and that power is available on all power pins.**

Power Up

If an unformatted floppy disk resides in a floppy drive connected to the VME board during power up, the VME board does not boot and the OpenBoot prompt does not appear. Therefore, never boot the VME board with an unformatted floppy disk residing in a floppy drive connected to the VME board.

Operation

While operating the board ensure that the environmental and power requirements are met:

- **To ensure that the operating conditions are met, forced air cooling is required within the chassis environment.**
- **High humdity and condensation on the surface cause short circuits. Only operate the board above 0 °C. Make sure the board is**

completely dry and there is no moisture on any surface before applying power.

Replacement/Expansion

Only replace or expand components or system parts with those recommended by Force Computers. Otherwise, you are fully responsible for the impact on EMC or any possible malfunction of the product.

Check the total power consumption of all components installed (see the technical specification of the respective components). Ensure that any individual output current of any source stays within its acceptable limits (see the technical specification of the respective source).

RJ-45 Connector

The RJ–45 connector on the front panel must only be used for twisted–pair Ethernet (TPE) connections. Connecting a telephone to such a connector may destroy your telephone as well as your board. Therefore:

- **Clearly mark TPE connectors near your working area as network connectors**
- **Only connect TPE bushing of the system to safety extra low voltage (SELV) circuits.**
- **Make sure that the length of the electric cable connected to a TPE bushing does not exceed 100 meter.**

If you have further questions, ask your system administrator.

Battery

If a lithium battery on the board has to be exchanged (see Appendix Battery Exchange), observe the following safety notes:

- **Wrong battery exchange may result in a hazardous explosion and board damage. Therefore, always use the same type of lithium battery as is installed and make sure the battery is installed as described.**
- **Exchanging the battery after seven years of actual battery use have elapsed results in data loss. Therefore, exchange the battery before seven years of actual battery use have elapsed.**

- **Exchanging the battery always results in data loss of the devices which use the battery as power backup. Therefore, back up affected data before exchanging the battery.**

Environment

Always dispose of used batteries and/or old boards according to your country's legislation, if possible in an environmentally acceptable way.

Sicherheitshinweise

Dieser Abschnitt enthält Sicherheitshinweise, die bei Einbau, Betrieb und Wartung des Boards zu beachten sind.

Wir sind darauf bedacht, alle notwendigen Informationen, die für die Installation und den Betrieb erforderlich sind, in diesem Handbuch bereit zu stellen. Da es sich jedoch bei dem Board um ein komplexes Produkt mit vielfältigen Einsatzmöglichkeiten handelt, können wir die Vollständigkeit der im Handbuch enthaltenen Informationen nicht garantieren. Falls Sie weitere Informationen benötigen sollten, wenden Sie sich bitte an die für Sie zuständige Geschäftsstelle von Force Computers.

Das Board erfüllt die für die Industrie geforderten Sicherheitsvorschriften und darf ausschliesslich für Anwendungen in der Telekommunikationsindustrie und im Zusammenhang mit Industriesteuerungen verwendet werden.

Einbau, Wartung und Betrieb dürfen nur von durch Force Computers ausgebildetem oder im Bereich Elektronik oder Elektrotechnik qualifiziertem Personal durchgeführt werden. Die in diesem Handbuch enthaltenen Informationen dienen ausschliesslich dazu, das Wissen von Fachpersonal zu ergänzen, können es aber in keinem Fall ersetzen.

EMV

Das Board wurde in einem Force Computers Standardsystem getestet. Es erfüllt die für digitale Geräte der Klasse A gültigen Grenzwerte in einem solchen System gemäß den FCC–Richtlinien Abschnitt 15 bzw. EN 55022 Klasse A. Diese Grenzwerte sollen einen angemessenen Schutz vor Störstrahlung beim Betrieb des Boards in Gewerbe– sowie Industriegebieten gewährleisten.

Das Board arbeitet im Hochfrequenzbereich und erzeugt Störstrahlung. Bei unsachgemäßem Einbau und anderem als in diesem Handbuch beschriebenen Betrieb können Störungen im Hochfrequenzbereich auftreten.

Warnung! Dies ist eine Einrichtung der Klasse A. Diese Einrichtung kann im Wohnbereich Funkstörungen verursachen. In diesem Fall kann vom Betreiber verlangt werden, angemessene Maßnahmen durchzuführen.

Wenn Sie das Board ohne PMC Modul verwenden, schirmen Sie freie Steckplätze mit einer Blende ab, um einen ausreichenden EMV Schutz zu gewährleisten. Wenn Sie Boards in Systeme einbauen, schirmen Sie freie Steckplätze mit einer Blende ab.

Schaltereinstellungen

Das Ändern der mit 'reserved' gekennzeichneten Schalter kann zu Störungen im Betrieb des Boards führen. Ändern Sie die Schaltereinstellungen der mit 'reserved' gekennzeichneten Schalter nicht, da diese Schalter mit produktionsrelevanten Funktionen belegt sein können, die im normalen Betrieb Störungen auslösen könnten.

Das Ändern der Schaltereinstellungen während des laufendes Betriebs kann das Board beschädigen. Prüfen und ändern Sie die Schaltereinstellungen, bevor Sie das Board installieren.

Installation

Elektrostatische Entladung und unsachgemäßer Ein– und Ausbau des Boards kann Schaltkreise beschädigen oder ihre Lebensdauer verkürzen. Beachten Sie deshalb die folgenden Punkte:

- **Berühren Sie das Board oder elektrische Komponenten in einem nicht ESD–geschützten Bereich, kann dies zu einer Beschädigung des Boards führen. Bevor Sie Boards oder elektronische Komponenten berühren, vergewissern Sie sich, dass Sie in einem ESD–geschützten Bereich arbeiten.**
- **Drücken Sie beim Ein– oder Ausbau des Boards nicht auf die Frontplatte, sondern benutzen Sie die Griffe.**
- **Lesen Sie vor dem Ein– oder Ausbau von zusätzlichen Geräten oder Modulen das dazugehörige Benutzerhandbuch.**
- **Vergewissern Sie sich, dass das Board über alle Stecker an die VME Backplane angeschlossen ist und alle Spannungskontakte mit Strom versorgt werden.**

Booten

Befindet sich während des Bootens eine unformatierte Diskette in einem mit dem VME Board verbundenen Diskettenlaufwerk, bootet das VME Board nicht, und die OpenBoot–Eingabeaufforderung

erscheint nicht. Booten Sie deshalb niemals das VME Board, wenn sich eine unformatierte Diskette in einem mit dem VME Board verbundenen Diskettenlaufwerk befindet.

Betrieb

Achten Sie darauf, dass die Umgebungs– und die Leistungsanforderungen während des Betriebs eingehalten werden:

- **Um zu gewährleisten, dass die Anforderungen während des Betriebs eingehalten werden, ist eine Luftkühlung notwendig**
- **Betreiben Sie das Board nur innerhalb der angegebenen Grenzwerte für die relative Luftfeuchtigkeit und Temperatur, da durch hohe Luftfeuchtigkeit Kurzschlüsse entstehen können. Stellen Sie vor dem Einschalten des Stroms sicher, dass sich auf dem Board kein Kondensat befindet und betreiben Sie das Board nicht unter 0 °C.**

Wenn Sie das Board in Gebieten mit starker elektromagnetischer Strahlung betreiben, stellen Sie sicher, dass das Board mit dem System verschraubt ist und das System durch ein Gehäuse abgeschirmt wird.

Stellen Sie sicher, dass Anschlüsse und Kabel des Boards während des Betriebs nicht versehentlich berührt werden können.

Austausch/Erweiterung

Verwenden Sie bei Austausch oder Erweiterung nur von Force Computers empfohlene Komponenten und Systemteile. Andernfalls sind Sie für mögliche Auswirkungen auf EMV oder Fehlfunktionen des Produktes voll verantwortlich.

Überprüfen Sie die gesamte aufgenomme Leistung aller eingebauten Komponenten (siehe die technischen Daten der entsprechenden Komponente). Stellen Sie sicher, dass die Stromaufnahme jedes Verbrauchers innerhalb der zulässigen Grenzwerte liegt (siehe die technischen Daten des entsprechenden Verbrauchers).

RJ-45 Stecker

Der RJ–45 Stecker auf der Frontblende darf nur für Twisted–Pair–Ethernet (TPE) Verbindungen verwendet werden.

Beachten Sie, dass ein versehentliches Anschließen einer Telefonleitung an einen solchen TPE Stecker sowohl das Telefon als auch das Board zerstören kann. Beachten Sie deshalb die folgenden Hinweise:

- **Kennzeichnen Sie TPE–Anschlüsse in der Nähe Ihres Arbeitsplatzes deutlich als Netzwerkanschlüsse.**
- **Schließen Sie an TPE–Buchsen ausschließlich SELV–Kreise (Sicherheitskleinspannungsstromkreise) an.**
- **Die Länge des mit dem Board verbundenen Twisted–Pair Ethernet–Kabels darf 100 m nicht überschreiten.**

Falls Sie Fragen haben, wenden Sie sich bitte an Ihren Systemadministrator.

Batterie

Muss eine Lithium–Batterie auf dem Board ausgetauscht werden (siehe Appendix Battery Exchange), beachten Sie die folgenden Sicherheitshinweise:

- **Fehlerhafter Austausch von Lithium–Batterien kann zu lebensgefährlichen Explosionen führen. Verwenden Sie deshalb nur den Batterietyp, der auch bereits eingesetzt wurde und befolgen Sie die Installationsanleitung.**
- **Verwenden Sie die Batterien länger als sieben Jahre, kann dies zu Datenverlusten führen. Tauschen Sie deshalb die Batterie aus, bevor sieben Jahre reiner Betrieb vorüber sind.**
- **Der Austausch der Batterie bringt immer einen Datenverlust bei den Komponenten mit sich, die sich durch die Batterie die Stromversorgung sichern. Sichern Sie deshalb vor dem Batterieaustausch Ihre Daten.**

Umweltschutz

Entsorgen Sie alte Batterien und/oder Boards stets gemäß der in Ihrem Land gültigen Gesetzgebung, wenn möglich immer umweltfreundlich.

1

Introduction

Features

The SPARC/CPU56 is a high–performance VME single–board computer based on the 650 MHz UltraSPARC IIi+ processor. It provides 512 MByte on–board SDRAM memory. Important features are:

- Two Wide Ultra3 SCSI interfaces via front panel
- One 10/100/1000 BaseT Ethernet interface via front panel and one via IOBP
- One 10/100 BaseT interface via front panel or IOBP
- Two serial RS–232 interfaces via front panel and two serial RS–232/RS–454 interfaces via IOBP
- Optional on–board hard disk
- Keyboard/Mouse interface via front panel or IOBP
- Floppy disk and parallel interface via IOBP
- One PMC slot
- Solaris 8/9 and VxWorks support

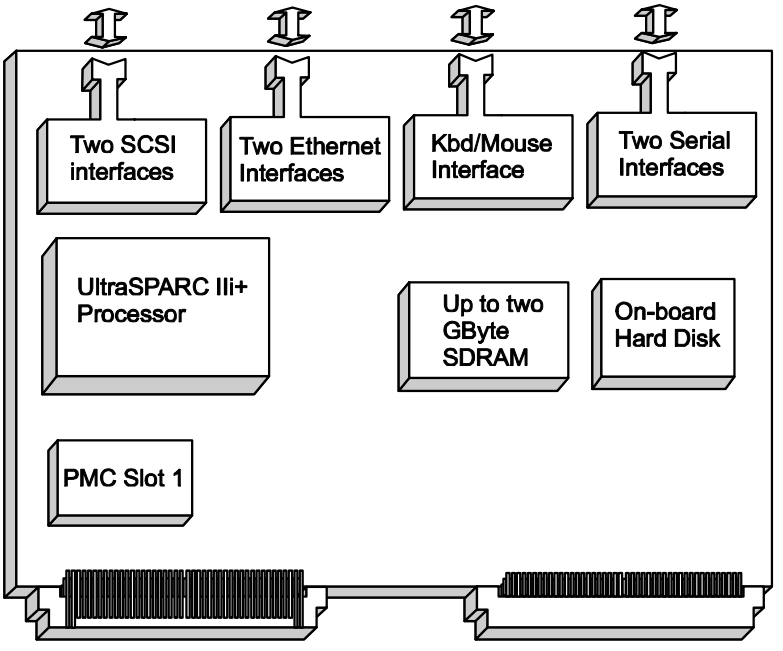


Figure 1: *Function Blocks*

Standard Compliances

The CPU board was designed to comply with the standards listed below.

Table 1: *Standard Compliances*

Standard	Description
IEC 68–2–1/2/3/13/14	Climatic environmental requirements.
IEC 68–2–6/27/32	Mechanical environmental requirements
EN 609 50/UL 1950 (predefined Force system); UL 94V–0/1	Legal safety requirements
EN 55022, EN 55024, FCC Part 15 Class A	EMC requirements on system level
ANSI/IPC_A–610 Rev. B Class 2 ANSI/IPC–R–700B ANSI–J–001...003	Manufacturing requirements
ISO 8601	Y2K compliance
NEBS Standard GR–63–CORE NEBS Standard GR–1089–CORE	NEBS level three

Ordering Information

When ordering board variants, hard- and software upgrades use the order numbers given below.

Product Nomenclature

In the following table you find the key for the product name extensions used for board variants.

Table 2: *Product Nomenclature*

SPARC/CPU-56/xxx-ccc-Lyyy-zz	
xxx	SDRAM capacity in MByte
ccc	CPU speed in MHz
Lyyy	L2-cache in KByte
zz	Flash memory size in MByte

Order Numbers

The table below is an excerpt from the board's ordering information. Ask your local Force Computers representative for the current ordering information.

Table 3: *Board Ordering Information*

Order No.	SPARC/CPU-56/...	Description
111327	512-650-L512-16	512 MByte SDRAM, 650 MHz CPU frequency, 512 KByte L2 cache and 16 MByte flash memory
121275	1024-650-L512-16	! GByte SDRAM, 650 MHz CPU frequency, 512 KByte L2 cache and 16 MByte flash memory

The table below is an excerpt from the board's accessories ordering information. Ask your local Force Computers representative for the current ordering information.

Table 4: *Board Accessories Ordering Information*

Order No.	Accessory	Description
111330	SPARC/IOBP-CPU-56/3	Three-row variant of CPU board's IOBP
111331	SPARC/IOBP-CPU-56/5	Five-row variant of CPU board's IOBP

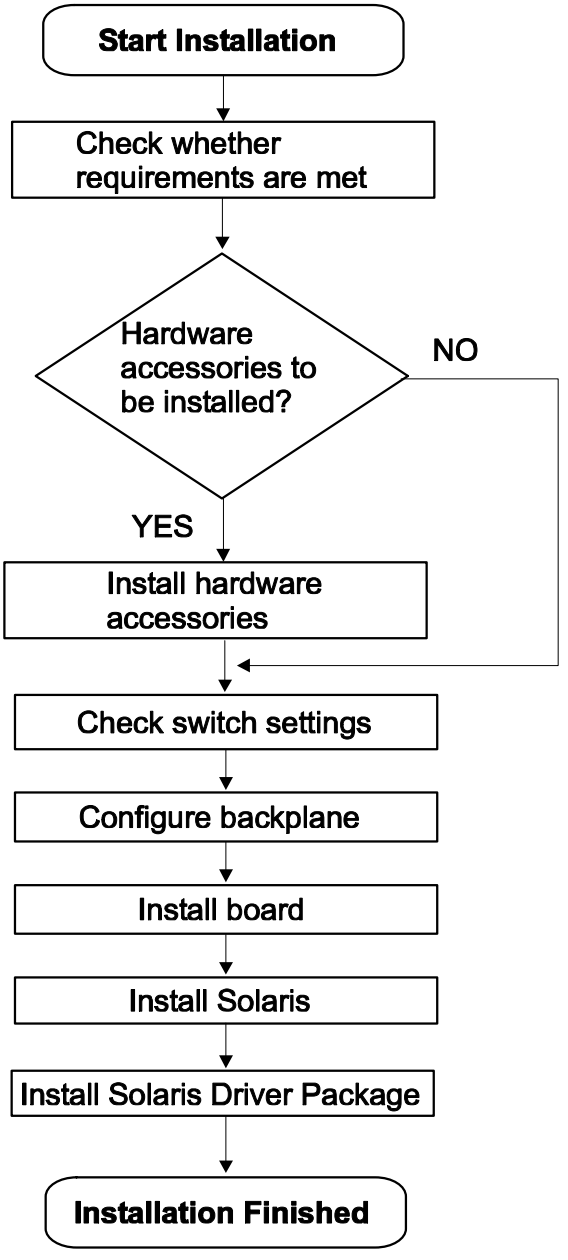
Order No.	Accessory	Description
111332	ACC/CABLE/SCSI-U160	SCSI-3-to-SCSI-4 adapter cable
120454	ACC/CABLE/RS422	RS232-to-RS422 serial adapter cable
109045	SPARC/MEM – 550/1024	Memory module with 1 GByte memory
107257	ACC/CABLE/KBDMSE/540	Splitter cable for PS2/SUN keyboard/mouse

2

Installation

Action Plan

In order to install the board, the following steps are necessary and will be described in further detail in the sections of this chapter.



Requirements

In order to meet the environmental requirements, the CPU board has to be tested in the system in which it is to be installed.

Before you power up the board, calculate the power needed according to your combination of board upgrades and accessories.

Environmental Requirements

The environmental conditions must be tested and proven in the used system configuration. The conditions refer to the surrounding of the board within the user environment.

Note: Operating temperatures refer to the temperature of the air circulating around the board and not to the actual component temperature.

- **Board damage**
  Operating the board in a chassis without forced air cooling may lead to board damage.
  When operating the board, make sure that forced air cooling is available.

- **Board damage**
  High humidity and condensation on the board surface causes short circuits.
  Do not operate the board outside the specified environmental limits. Make sure the board is completely dry and there is no moisture on any surface before applying power. Do not operate the board below 0˚C.

Table 5: *Environmental Requirements*

Feature	Operating	Non-Operating
Temperature	0 ˚C to +50 ˚C	-40 ˚C to +85 ˚C
Forced airflow	300 LFM (linear feet per minute)	-
Temp. change	+/- 0.5 ˚C/min	+/- 1.0 ˚C/min
Rel. humidity	5% to 95% non-condensating at +40 ˚C	5% to 95% non-condensating at +40 ˚C
Altitude	-300 m to + 3,000 m	-300 m to + 13,000 m

Feature	Operating	Non–Operating
Vibration		
10 to 15 Hz 15 to 150 Hz	2 mm amplitude 2 g	5 mm amplitude 5 g
Shock	5g/11 ms halfsine	15g/11 ms halfsine
Free fall	100 mm / 3 axes	1,200 mm / all edges and corners (packed state)

Power Requirements

The board power requirements depend on the installed hardware accessories. In the following table you will find typical examples of power requirements without any accessories installed. If you want to install accessories on the board, the load of the respective accessory has to be added to that of the board. For information on the accessories' power requirements, refer to the documentation delivered together with the respective accessory or consult your local Force Computers representative for further details.

Table 6: *Power Requirements*

Requirement	5V	12V
Minimum Voltage	4.88V	11.64V
Typical Voltage	5V	12V
Maximum Voltage	5.25V	12.6V
Typical Current	4.7A	1.5A
Maximum Current	5.7A	1.63A
Typical Power Requirement	25W	18W
Maximum Power Requirement	30W	20W

Note: The CPU board only powers up if the 5V and 12V supply voltages are stable and within their limits. However, there are systems which are not fully VMEbus–compliant. The power supplies of these systems do not turn on the 12V supply if the 5V supply has not been loaded before. Use a VMEbus board which loads the 5V in these systems to avoid a power–up deadlock situation.

Hardware Accessories

The following upgrades and accessories are available for the CPU board:

- IOBP
- Memory modules
- PMC modules
- Hard disk
- SCSI–U160 cable
- RS–422 serial cable
- PS2 splitter cable

IOBP

As a separate price list item an I/O back panel is available for the CPU board, the IOBP–CPU–56. It is available in two variants which differ in the number of VMEconnector rows: the three–row variant IOBP–CPU–56–3 and the five–row variant IOBP–CPU–56–5. The interfaces available via both IOBP variants are:

- IDE
- 10/100Base–TX Ethernet
- Parallel
- Two USB
- Two serial (RS–232 and RS–422)

In addition to these interfaces, the five–row variant IOBP–CPU–56–5 provides:

- Keyboard/mouse interface (SUN or PS/2 style)
- Third USB interface
- Floppy interface
- 10/100/1000 Base–TX Ethernet

For further information on the IOBP and its installation, refer to the *SPARC/IOBP–CPU–56 Installation Guide*.

Caution

Board Damage
Using the CPU board together with an IOBP for which it is not designed, may destroy the board.
Only use the CPU board together with the IOBP-CPU-56.

Memory Modules

The main memory capacity is adjustable via installation of the Force Computers SPARC/MEM-550 memory upgrade module. It offers 1 GByte additional memory space.

For installation information, refer to the *SPARC/MEM-550 Installation Guide*.

PMC Module

The SPARC/CPU-56 provides one PMC slot. It supports a 64-bit data bus with a frequency of 33 MHz.

Note: The used PMC modules must be compliant with the safety regulations of the country where the equipment is installed.

The corresponding PMC connectors are shown in the figure below.

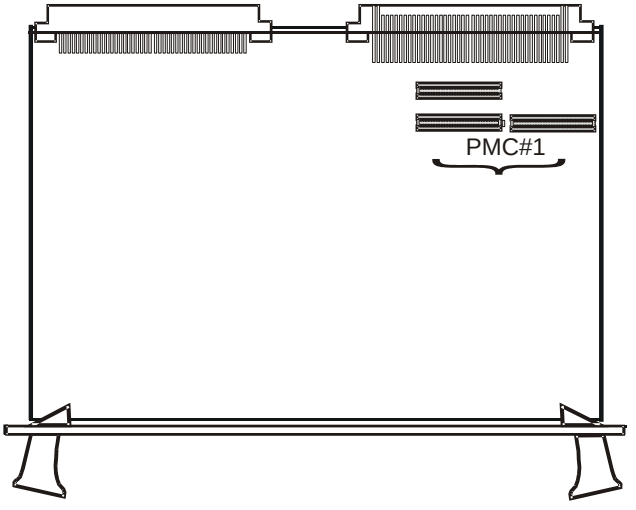


Figure 2: *PMC Connectors*

Note:

- **To ensure proper EMC shielding, either operate the board with a PMC module installed or with a blind panel.**

- **If the board is upgraded with a PMC module, ensure that the blind panel is stored in a safe place in order to be reused again when removing the PMC module.**
- **Processor PMC modules are only supported in non–monarch mode.**

The signaling level is determined via a voltage key which has to be installed into one of two holes that are assigned to this PMC slot. One hole corresponds to a signaling level of 5V, the other to a signalling level of 3.3V. Depending on the hole the voltage key is installed into, the signaling level is set accordingly.

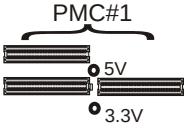
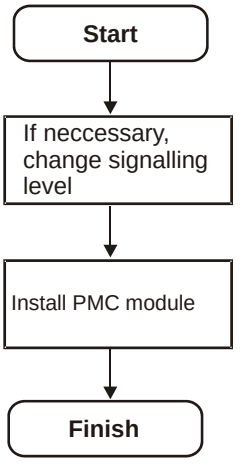


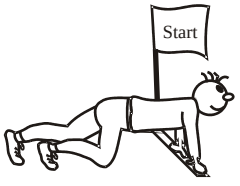
Figure 3: *Location of PMC Voltage Keys*

By default the signalling level is set to 5V.

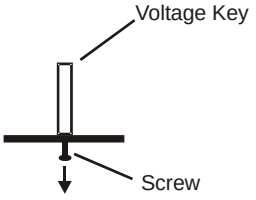
Installalling a PMC Module



Changing Signalling Level

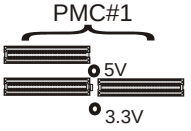


1. Remove screw which fixes the voltage key to board

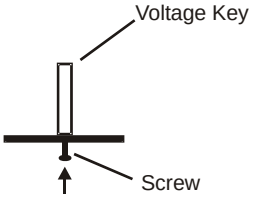


2. Remove voltage key

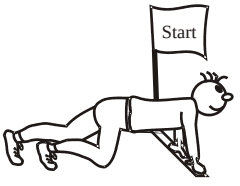
3. Place voltage key into hole which corresponds to desired signalling level



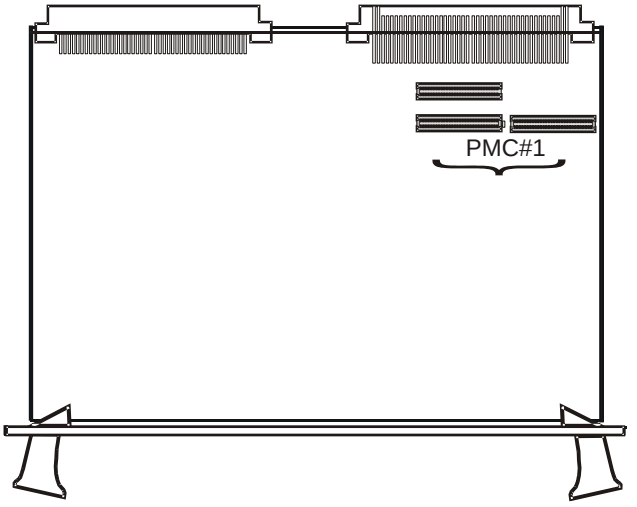
4. Fix voltage key to board by fastening screw



Installing the PMC Module



1. Plug PMC module into PMC connectors



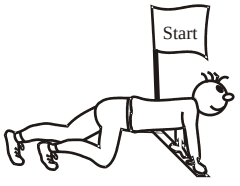
Caution

PMC Module Damage
If the power of the PMC module exceeds 7.5W, the board and the PMC module are damaged
Make sure the total power consumption at +/–12V, 5V and 3.3V level does not exceed 7.5 W. Make also sure that the current at the +12V power supply does not exceed 100mA.

2. Make sure standoffs of PMC module cover mounting holes of the board
3. Place screws delivered with PMC module into mounting holes
4. Fasten screws

Removing a PMC Module

Procedure



1. Remove screws
2. Disconnect PMC module carefully from slot

3. Close front panel gap with blind panel

Hard Disk

A hard disk is available for the CPU board on request. It can be connected to the IDE1 interface which is accessible via an on-board connector.

The installation of the hard disk is described in the Installation Guide delivered together with the hard disk.

SCSI-U160 Cable

The SCSI-U160 cable is available as accessory kit called ACC/CABLE−SCSI−U160. It provides a SCSI U160 cable with a length of three meters which has one SCSI−3 and one SCSI−4 connector at its ends. It can be used to connect SCSI devices to the CPU board. For details, refer to the *ACC/CABLE/SCSI-U160 Installation Guide* which is delivered together with the accessory kit.

RS-422 Cable

The RS-422 cable is available as accessory kit called ACC/CABLE−RS−422 and provides a serial cable with a length of 2.6 meters that has one male DSub9 RS−422 and one female mini DSub9 RS−232 connector at its ends. It allows to connect RS−422 devices to the serial B interface of the CPU board. For details, refer to the *ACC/CABLE/RS-422 Installation Guide*which is delivered together with the accessory kit.

PS/2 Splitter Cable

The PS/2 splitter cable can be connected to the SUN-type keyboard/mouse connecter of the CPU board or its IOBP. It allows to operate a PS/2-style keyboard and mouse.

Switch Settings

Caution

Board Damage
Setting/resetting the switches during operation causes board damage. Therefore, check and change switch settings before you install the board.

The CPU board provides four configuration switches: SW1, SW2, SW3 and SW4.

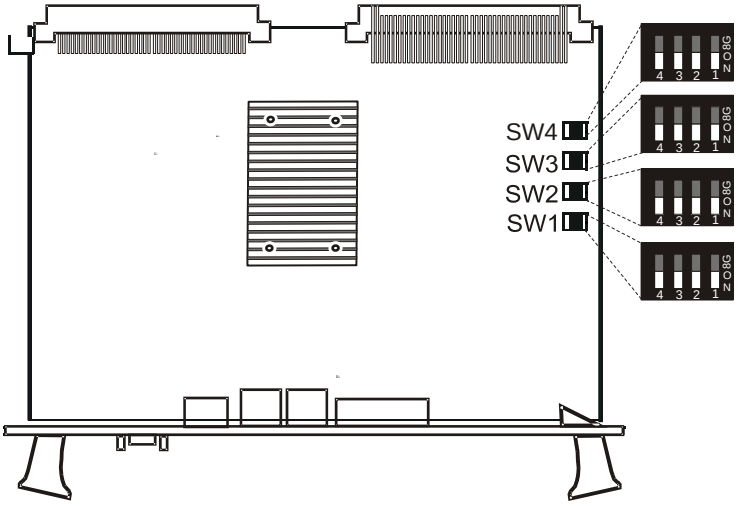


Figure 4: *Location of Switches on Board's Top Side*

Table 7: *Switch Settings*

Switch	No.	Description
SW1	1	Flash memory write protection OFF (default): Flash memory writing disabled ON: Flash memory writing enabled
	2	Boot device selection OFF (default): Boot from PLCC PROM ON: Boot from flash memory device
	3	Enable watchdog OFF (default): Watchdog disabled ON: Watchdog enabled
	4	Enable reset/abort key OFF (default): reset/abort key enabled ON: reset/abort key disabled
SW2	1..4	User defined switches. For detailed information refer to section "Switch 1 and 2 Status Register".

Switch	No.	Description
SW3	1	Enable Termination for SCSI 1 OFF (default): Termination enabled ON: Termination disabled
	2	Enable termination for SCSI 2 OFF (default): Termination enabled ON: Termination disabled
	3	Enable termination for SCSI 3 (on I/O-board, if applicable) OFF (default): Termination enabled ON: Termination disabled
	4	Reserved
SW4	1..2	VME Slot 1 Detection SW4-1 OFF (default): Automatic VMEbus slot 1 detection enabled SW4-1 ON and SW4-2 OFF: VME slot 1 function enabled SW4-1 ON and SW4-2 ON: VME slot 1 function disabled
	3	External VMEbus SYSRESET function OFF (default): VMEbus SYSRESET generates on-board RESET ON: VMEbus SYSRESET does not generate on-board RESET
	4	VMEbus SYSRESET generation OFF (default): On-board reset is driven to VMEbus SYSRESET ON: On-board reset is not driven to VMEbus SYSRESET

Board Installation

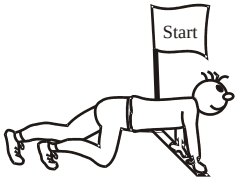
Board Damage
Installing the board into a powered system may damage this and other boards in the system.
Only install the board into a non-powered system.

Backplane Configuration

If the CPU board is plugged into slot 1 and configured accordingly with switch SW4 (refer to "Switch Settings" table), the board acts as IACK daisy-chain driver. Plugged in any other slot, the board closes the IACKIN-IACKOUT path.

If one board is missing in this daisy chain, an active backplane will be able to automatically transfer the signals to the next board in the chain. If the board is not plugged into an active backplane, jumpers on the backplane will transmit the signals. The jumpers have to be set manually.

Configuration Procedure



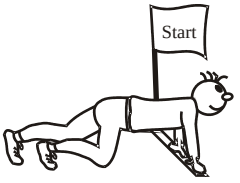
1. Remove jumpers connecting BG3IN# and BG3OUT# signals from empty slot on backplane where the CPU board is to be plugged into backplane
2. Assemble jumpers for BG3IN# and BG3OUT# signals on lower and higher slots on backplane where no board is plugged to ensure that daisy chain is not interrupted

If configured accordingly, the CPU board recognizes automatically whether it is plugged into slot 1 of the VMEbus backplane or in any other slot. This auto-configuration feature requires SW4-2 to be set to the OFF position. The VMEbus system controller is enabled via auto-configuration if the CPU board is plugged into slot 1. Otherwise, it is disabled.

If more than one system controller is active in the VMEbus system, the board or other VMEbus participants can be damaged. Therefore, always ensure that only one CPU board is configured to be system controller in the VMEbus system.

Installing the CPU Board

Procedure



1. Check system documentation for all important steps to be taken before switching off power
2. Take those steps
3. Switch off power
4. Plug board into system slot on left–hand side

Note: Make sure all other boards which are plugged into the system are to the right of the system board.

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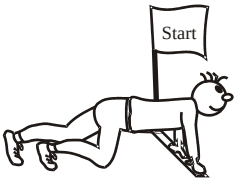
5. Fasten board with screws
6. Plug interface cables into front panel connectors, if applicable
7. Switch on power

Removing the CPU Board

Procedure



1. Check system documentation for all important steps to be taken before switching off power
2. Take those steps
3. Switch off power
4. Remove interface cables, if applicable
5. Unfasten screws
6. Remove board

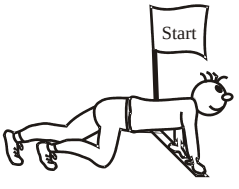
Powering Up

We recommend to use a terminal when powering up the CPU board. The advantage of using a terminal is that you do not need any frame buffer, monitor, or keyboard for initial power up.

Note:

- **Before powering up, check the "Requirements" section for installation prerequisites and requirements.**
- **If an unformatted floppy disk resides in a floppy drive connected to the CPU board during power up, the CPU board does not boot and the OpenBoot prompt does not appear.**
- **Check the consistency of the switch settings ("Switch Settings" table).**

Power Up Procedure



1. Connect terminal to front panel serial I/O interface A
   For information on the serial interface connector pinout, see "On-Board Connectors of the CPU Board" section.
2. Switch on system

The monitor will display information about the OpenBoot booting process.

3. Enter OpenBoot commands, if applicable

PLCC PROM and Flash Memory Device

By default, the CPU board boots from the 1 MByte PLCC PROM which is not writeable and contains the OpenBoot firmware. Alternatively, a 16 MByte flash memory device can be enabled with SW2–1..4 to boot from it and to store user applications.

Installing Solaris

The CPU board is designed to run with Solaris 8 2/02 or higher with the 64–bit kernel and with Solaris 9. Pay attention to the guidelines in this section before and during Solaris installation.

Note: Solaris versions prior to version 8 2/2 are not supported. The CPU board runs with 64–bit kernel only.

The following devices of the CPU board are not supported by the Solaris operating system:

- Universe II PCI–to–VMEbus bridge
- On–board flash memory
- Temperature sensors, LEDs, timers and watchdog
- Intel 82540EM Ethernet device
- IDE device error handling

If you wish to use one of these devices, you need to install the Force Computers Solaris Driver Package. Details will be given in the following sections.

If you want to use PS/2 keyboard and mouse, you have to customize the following software groups during the Solaris installation:

- Developer system support
- End user system support

- Core system support

The customization consists of selecting ”PS/2 keyboard and mouse device drivers (Root, 64 Bit) under ”drivers for SME support (64 Bit)”.

The remaining software groups do not require customization.

Note: During installation, make sure that the 64–bit support is enabled.

If Solaris is already installed and you want to have PS/2 support afterwards, you have to install the SUNWkmp2x for 64–bit package.

Note: During the Solaris installation you may get the following Solaris error message: ”Could not reset the IDE core of SouthBridge”. If this happens, try to install Solaris from another CD–ROM drive or from a SCSI CDROM drive.
After the Solaris installation has finished, this Solaris error message can be avoided by installing the Solaris Driver Package FRCcpu56pm.

For audio I/O and IDE ATA 100 support, you have to install Solaris patches. The following table provides details.

Table 8: *Solaris Patches*

Supported Device	Solaris Version	Patch
Audio I/O (if applicable)	8	109896–17 or newer
	9	Currently not supported. A patch will be available in the near future.
IDE ATA 100	8	108974–31 or newer
	9	112954–03 or newer

Solaris Driver Package

Force Computers provides a Solaris driver package which supports the following devices and features of the CPU board:

- Universe II PCI–to–VMEbus bridge
- On–board flash memory
- Temperature sensors, LEDs and watchdog

- Intel 82540EM GBit Ethernet device
- CPU-56 platform mode friver for IDE device error handling

If you wish to use one of these devices you need to install the Force Computers Solaris Driver Package Version 2.20.

For a detailled description of how to install and use it, refer to the *Solaris Driver Package Rel. 2.20 Installation and Reference Guide* which can be downloaded from the Force Computers S.M.A.R.T. server.

The following table shows which driver has to be installed for a particular device.

Table 9: *Devices and Their Appropriate Drivers*

Device	Driver Name
Intel 8254xEM GBit Ethernet controller	FRCgei
Universe II PCI-to-VMEbus bridge	FRCvme
On-board flash memory	FRCflash
Temperature sensors, LEDs and watchdog	FRCctrl
IDE device (error handling)	FRCplatmod

Further information on these drivers is given in the following sections.

FRCgei

The assignment of the driver's instance number to an Intel 8254xEM GBit Ethernet device can be viewed by booting with the OpenBoot command boot -v. Each device is shown with the driver name and instance number during the Solaris boot up.

The other way to obtain the instance number of the Ethernet devices is to look into the file /etc/path_to_inst. In order to do so, type the following: **`grep fciprb /etc/path_to_inst`**

A typical output could be:

```
"/pci@1f,0/ethernet@2" 1 "frcgei"

"/pci@1f,0/pci@/ethernet@1" 0 "frcgei"
```

The first part in quotation marks specifies the hardware node name in the device tree. The number specifies the instance number and the third part also in quotation marks specifies the driver name.

The following table shows how the hardware node names are assigned to a label on the front panel and the IOBP-CPU-56.

Label	Location	Hardware Node
ETHERNET1/3	CPU front panel or IOBP-CPU-56	Standard Solaris eri Ethernet device
ETHERNET2	CPU front panel	/pci@1f,0/pci@4/ethernet@1
ETHERNET4	IOBP-CPU-56	/pci@1f,0 ethernet@2

The following table shows how the driver instance numbers are typically assigned to Ethernet devices on the CPU board.

Label	Location	Driver/Instance Number
ETHERNET1/3	CPU front panel or IOBP-CPU-56	eri0
ETHERNET2	CPU front panel	frcgei1
ETHERNET4	IOBP-CPU-56	frcgei0

FRCvme

The FRCvme is a set of drivers which handles the Universe II device. The following functions are supported:

- Master windows
- Slave windows
- Interrupts
- DMA controller
- VME arbiter
- Mailboxes

Additionally, the FRCvme package provides a common programming interface for application and driver development.

For more detailed information and board-specific notes, refer to the *Solaris Driver Package Installation and Reference Guide* and the *Solaris VMEbus Driver Programmer's Guide*.

FRCflash

The Solaris 2.x flash memory driver provides access to the flash memory device. Depending on the CPU board's switch settings, the flash memory is accessible as one user flash or is divided into a boot and a user section.

The following table shows the effects the different CPU board switch settings have on the flash segmentation and the flash write protection.

Table 10: *Flash Segmentation and Write Protection*

SW1–1 Setting	SW1–2 Setting	Flash Segmentation/Write–Protection	Boot from
OFF	OFF	16 MByte user flash, write–protected	PLCC PROM
ON	OFF	16 MByte user flash, not write–protected	PLCC PROM
OFF	ON	1 MByte boot flash + 15 MByte user flash, write–protected	Flash memory device
ON	ON	1 MByte boot flash + 15 MByte user flash, not write–protected	Flash memory device

FRCctrl

The FRCctrl driver contains the sysconfig device driver which offers the following features:

- Sets all user LEDs
- Accesses the temperature sensor devices
  To enable the temperature sensors, set the OpenBoot environment variable env–monitor before booting. To do so, enter at the prompt:
  `setenv env-monitor enabled`
- Enables and triggers watchdog functions
  To enable the watchdog, set switch SW1–3 to ON
- Increases the volume of a headphone (if applicable)

FRCplatmod

This driver ensures proper error handling for IDE devices. It should be installed immediately after the Solaris installation has been completed.

If this driver is not installed, the system may send error messages or can panic in case of IDE error handling.

3

Controls, Indicators, and Connectors

Front Panel

The following figure shows the connectors, keys and LEDs available on the front panel of the CPU board.

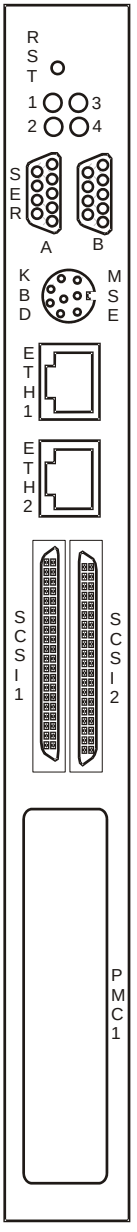


Figure 5: *Front Panel*

LEDs

All four LEDs available at the front panel are multi-purpose LEDs. Depending on the values contained in the LED control registers 1 to 4, they indicate either the board status or different network activities. Furthermore, all LEDs can be operated in user LED mode. For details about the LED control registers, refer to chapter “Maps and Registers”.

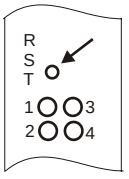
Table 11: *Description of Front Panel LEDs*

LED	Description
1	**Board Status (default)** Red: Board reset Weak red (on pressing the RST key): Board abort Weak red (during operation): 12V power supply on VME backplane not within its limits Green: Board running Blinking red/weak red: No PCI activity within last two seconds Blinking green: No boot code found Blinking weak red: 5V power supply on VME backplane not within its limit **IDE Activity** Depending on LED control register 1 settings, the LED indicates the activity of IDE 1 or IDE 2. **Ethernet Activity** Depending on LED control register 1 settings, the LED indicates activity of Ethernet interfaces 1 to 4 or a combination of these **User-LED Mode** Via LED control register 1, the LED can be programmed to be OFF, green or red.
2	**User-LED Mode (default)** Via LED control register 2 the LED can be programmed to be red, green or OFF. Furthermore it can be programmed to be blinking green or blinking red with different blinking frequencies. By default, the LED is OFF. **Ethernet Activity** Depending on LED control register 2 settings, the LED indicates activity of Ethernet interfaces 1 to 4 or a combination of these

LED	Description
3	**VME Bus Activity (default)** Red: Universe II asserted VME SYSFAIL signal to the VMEbus Green: Universe II accesses the VMEbus as master OFF: No SYSFAIL signal asserted and no Universe PCI–to–VME bridge activity **Ethernet Activity** Depending on LED control register 3 settings, the LED indicates activity of Ethernet interfaces 1 to 4 or a combination of these **User–LED Mode** Via LED control register 3, the LED can be programmed to be OFF, green or red.
4	**User–LED Mode (default)** Via LED control register 4, the LED can be programmed to be red, green or OFF. Furthermore, it can be programmed to be blinking green or blinking red with different blinking frequencies. By default, the LED is OFF. **Ethernet Activity** Depending on LED control register 4 settings, the LED indicates activity of Ethernet interfaces 1 to 4 or a combination of these.

Key

The front panel of the CPU board provides one key.



This key has two functions. When pressed longer than 0.5 s, a reset is generated which is indicated by the LED 1 shining red. When the key is pressed for a period shorther than 0.5 s, an abort is generated which is indicated by the LED 1 shining weak red.

Note: An abort should only be triggered if an application under Solaris or OpenBoot hangs. Do not trigger an abort to enter OpenBoot or to bypass the diagnostic routine during power up. After triggering an abort , the board is in diagnostic mode and the OpenBoot ok prompt appears. In this mode, you can diagnose what caused the program to hang. However, the board is not fully initialized and therefore is not fully functional. To regain the full functionality, you need to trigger a reset.

Connectors

The board provides the following connectors at its front panel:

- Serial
- Keyboard/Mouse
- Ethernet
- SCSI

Serial I/O

Two serial RS–232 interfaces A and B are available via two Mini D–Sub 9 connectors. Their pinouts are given below.

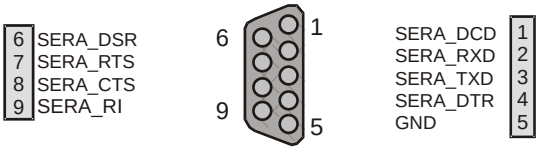


Figure 6: *Serial A Connector Pinout*

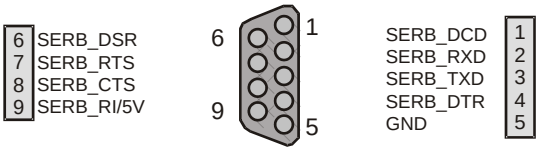


Figure 7: *Serial B Connector Pinout*

The signal provided by pin 9 of serial interface B depends on the value of the OpenBoot variable tty–rs422–enable?. If it is set to true, pin 9 holds 5V and serves as power feed for the ACC/CABLE/RS–422 cable connected to this interface. If the OpenBoot variable tty–rs422–enable? is set to false, pin 9 holds the signal SERB_RI and the serial interface B is a standard RS–232 interface.

Keyboard/Mouse

A SUN–type keyboard/mouse can be connected via an 8–pin Mini DIN connector. Its pinout is given below.

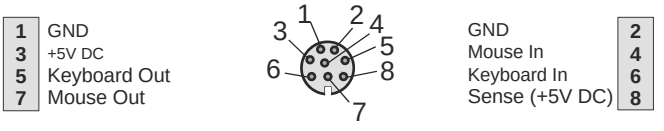


Figure 8: *SUN–Type Keyboard/Mouse Connector Pinout*

If you use an PS/2 splitter adapter cable, two PS/2 interfaces are available. One PS/2 interface can be used for connecting a keyboard, the second for connecting a mouse. Their respective pinouts are given below.

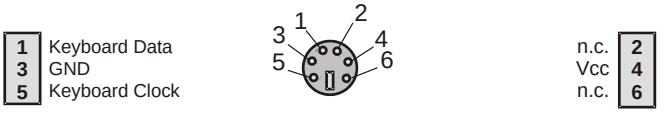


Figure 9: *PS/2 Keyboard Connector Pinout*

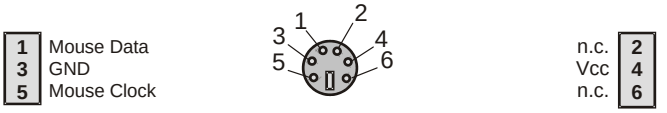


Figure 10: *PS/2 Mouse Connector Pinout*

Ethernet

Ethernet 1 and 2 are available via two RJ–45 connectors. Ethernet 1 is of type 10/100BaseT and Ethernet 2 of type 10/100/1000BaseT. The respective pinouts are given below.

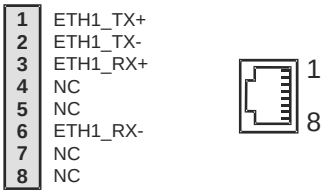


Figure 11: *Ethernet 1 Connector Pinout*

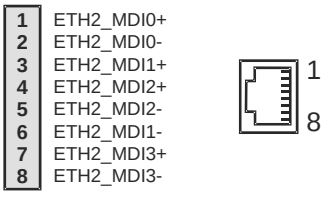


Figure 12: *Ethernet 2 Connector Pinout*

Note: The Ethernet 1 interface is also accessible as Ethernet 3 via the IOBP–CPU–56 . Both interfaces can not be accessed at the same time. The selection is made automatically by OpenBoot when booting the board and cannot be reversed anymore until the board is rebooted.

SCSI

Two SCSI interfaces 1 and 2 are available via two mini 68–pole SCSI4 connectors. Their pinout is given below.

1	SCSIx_D12+			SCSIx_D12-	35
2	SCSIx_D13+			SCSIx_D13-	36
3	SCSIx_D14+			SCSIx_D14-	37
4	SCSIx_D15+			SCSIx_D15-	38
5	SCSIx_DP1+			SCSIx_DP1-	39
6	SCSIx_D0+			SCSIx_D0-	40
7	SCSIx_D1+			SCSIx_D1-	41
8	SCSIx_D2+			SCSIx_D2-	42
9	SCSIx_D3+			SCSIx_D3-	43
10	SCSIx_D4+			SCSIx_D4-	44
11	SCSIx_D5+	1	35	SCSIx_D5-	45
12	SCSIx_D6+			SCSIx_D6-	46
13	SCSIx_D7+			SCSIx_D7-	47
14	SCSIx_DP0+			SCSIx_DP0-	48
15	GND			GND	49
16	DIFFSENSE			GND	50
17	TERMPWR			TERMPWR	51
18	TERMPWR			TERMPWR	52
19	n.c.			n.c.	53
20	GND			GND	54
21	SCSIx_ATN+			SCSIx_ATN-	55
22	GND			GND	56
23	SCSIx_BSY+			SCSIx_BSY-	57
24	SCSIx_ACK+	34	68	SCSIx_ACK-	58
25	SCSIx_RST+			SCSIx_RST-	59
26	SCSIx_MSG+			SCSIx_MSG-	60
27	SCSIx_SEL+			SCSIx_SEL-	61
28	SCSIx_CD+			SCSIx_CD-	62
29	SCSIx_REQ+			SCSIx_REQ-	63
30	SCSIx_IO+			SCSIx_IO-	64
31	SCSIx_D8+			SCSIx_D8-	65
32	SCSIx_D9+			SCSIx_D9-	66
33	SCSIx_D10+			SCSIx_D10-	67
34	SCSIx_D11+			SCSIx_D11-	68

Figure 13: *SCSI 1/2 Connector Pinouts*

Note: By default the SCSI termination is switched ON for SCSI interface 1 and 2. It can be switched OFF via switches. For details, see section "Switch Settings".

On-Board Connectors

The following connectors are on–board:

- VME
- PMC
- Memory Module
- IDE

PMC

The CPU board provides the PMC connectors P11, P12 and P13. They correspond to PMC slot 1.

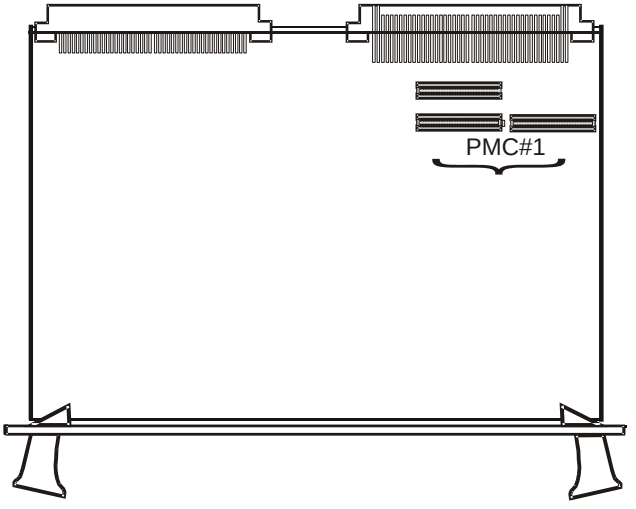


Figure 14: *Location of PMC Connectors*

These connectors provide access to an 64–bit/33 MHz PMC bus.

Memory Module

The CPU board provides the memory module connectors P8 and P9.

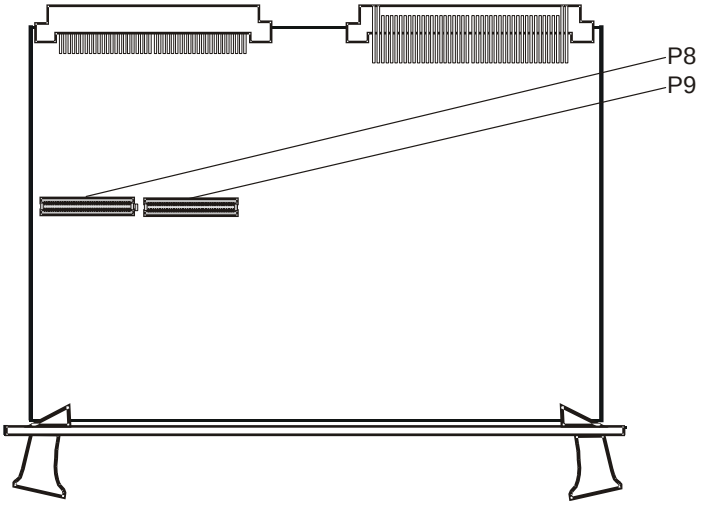
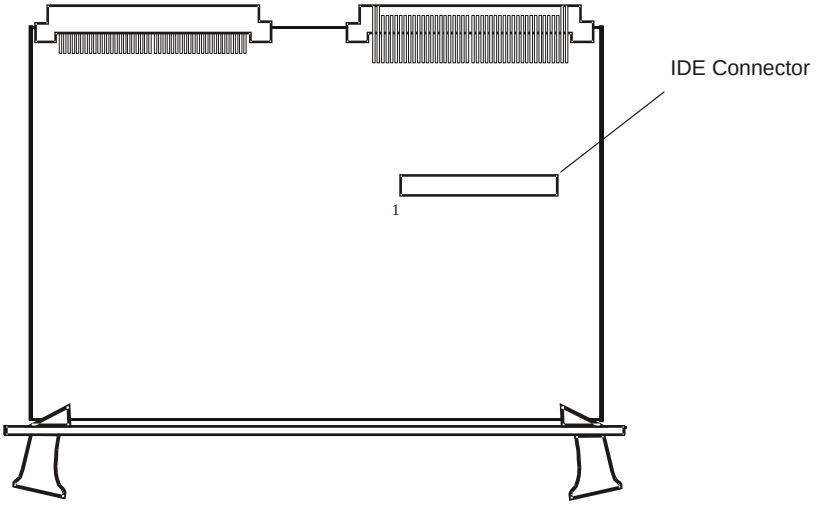


Figure 15: *Location of Memory Module Connectors*

IDE

The CPU board provides one IDE connector which provides access to IDE1.



Its pinout is given below.

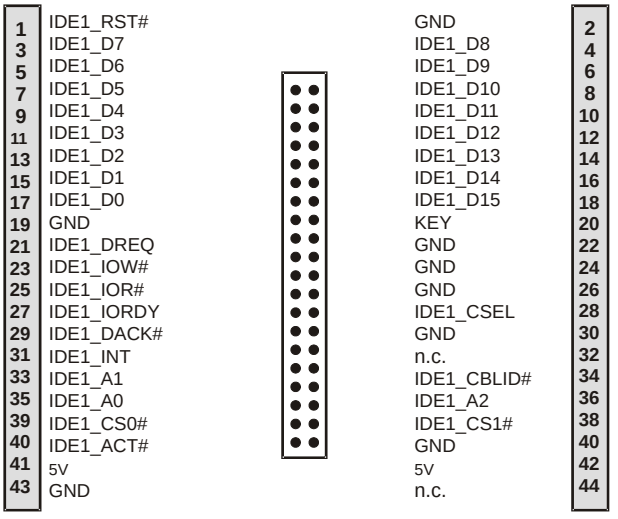


Figure 16: *IDE Connector Pinout*

VME

The CPU board provides the VME connectors P1 and P2.

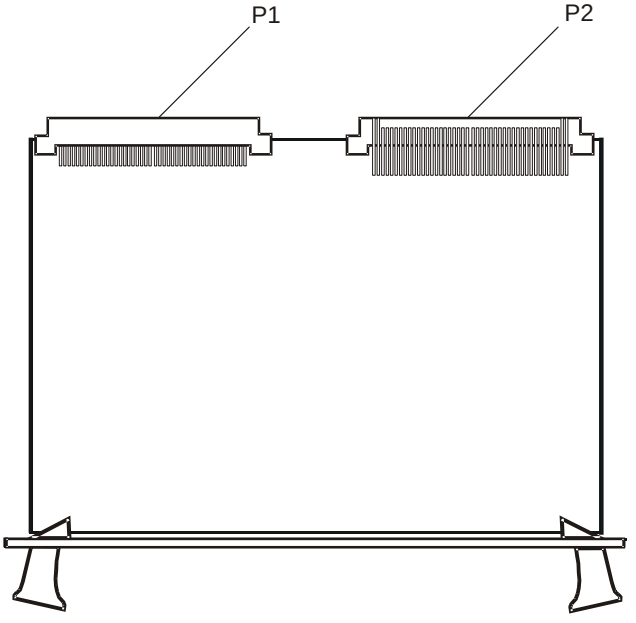


Figure 17: *Location of VME Connectors*

P1 carries standard VME signals and is therefore not further described in this guide.

P2 carries the following Force Computers specific signals:

- 10/100Mbit Ethernet 3 (ETH3)

- IDE (IDE2)
- Parallel (PAR)
- Serial (SERC, SERD)
- USB 1 and 2 (USB1, USB2)
- 10/100/1000 Mbit Ethernet 4 (ETH4)
- Floppy (FDC)
- USB 3 and 4 (USB3, USB4)
- SUN or PS/2 keyboard/ mouse interface (KBD)
- I2C (SMB)

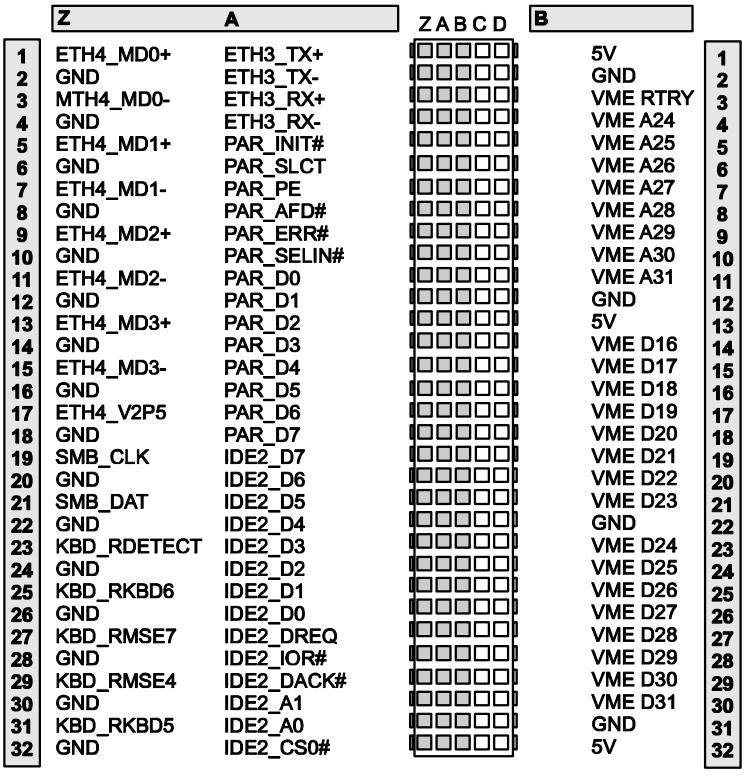


Figure 18: *P2 VMEbus Connector Pinout Rows Z – B*

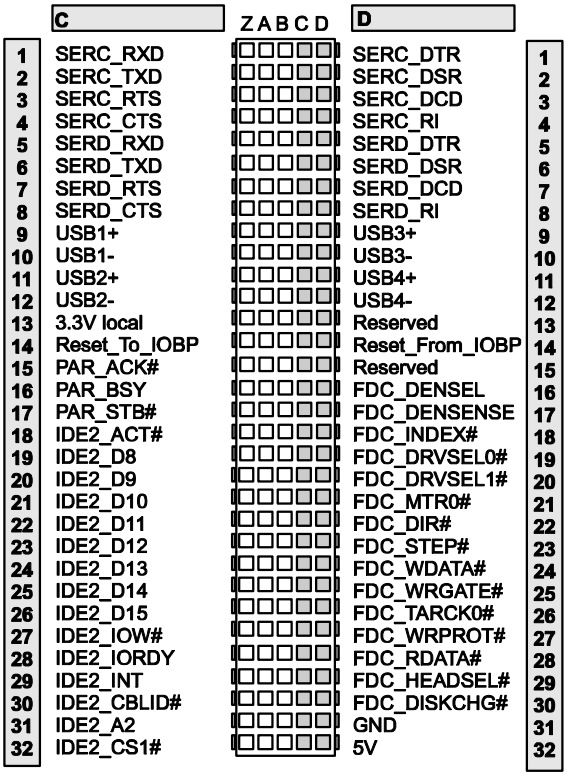


Figure 19: *P2 VMEbus Connector Pinout Rows C + D*

4

Devices' Features and Data Paths

Block Diagram

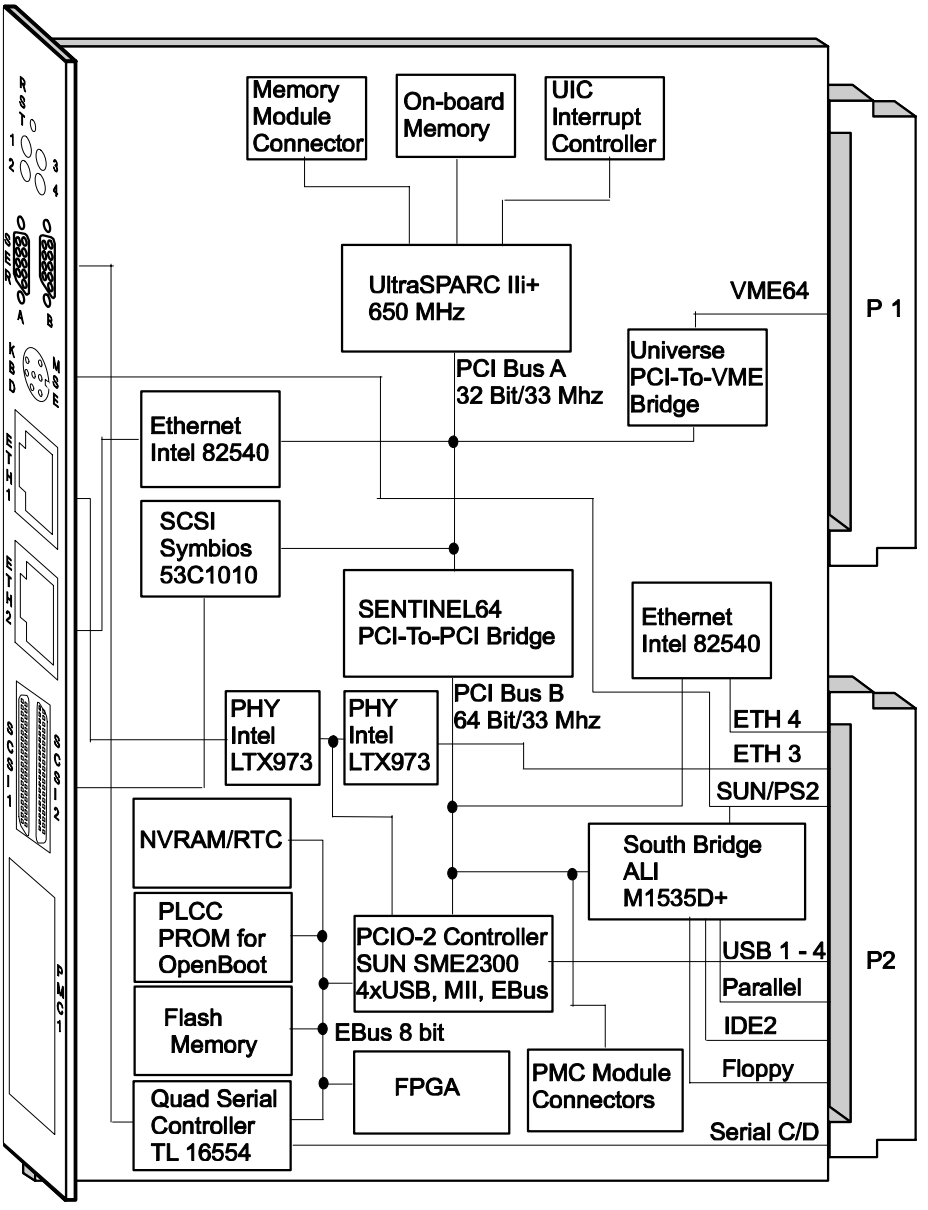


Figure 20: *Block Diagram*

UltraSPARC IIi+ Processor

The UltraSPARC IIi+ processor is based on the SPARC V9 architecture with VIS instruction set and supports up to 4 GByte of memory. Important features are:

- 650 MHz frequency
- Four-way superscalar processor
- 64-bit data paths
- 64-bit address arithmetic
- 41-bit virtual addressing
- 16 KByte instruction cache
- 16 KByte non-blocking primary data cache
- 512 KByte second level cache
- Sensors for observing CPU on-die temperature

Interrupt Controller

The UltraSPARC–IIi+ provides a 6–bit wide interrupt vector for 63 interrupt sources.

The UPA interrupt concentrator (UIC) provides the inputs for all necessary interrupts. It monitors all interrupts using a round–robin scheme with 33 MHz, converts them to a device–own vector and transmits this vector to the processor. The PCI interrupts engine (PIE) reflects every vector in one state bit. From the state bit a new vector is generated and transmitted to the processor's execution unit. If more than one interrupt state bit is active, the transmitting sequence of the new interrupt vector is priority controlled.

Every interrupt routed to the interrupt controller can be enabled or disabled separately in the interrupt source and in the processor.

PCI Bus A

PCI bus A is the primary PCI bus. It runs at 33 MHz and is 32 bit wide. The following devices are connected to it:

- Ethernet controller
- SCSI controller
- SENTINEL64 PCI–to–PCI bridge
- Universe

Ethernet Controller

The used Ethernet controller is an Intel 82540. It corresponds to Ethernet interface 2 available via the front panel and supports 10/100/1000BaseT Ethernet. Further important features are:

- Integrated PHY in a small package (uBGA196)
- Compatibility with IEEE 802.3/Ethernet
- DMA capability
- Interrupt generation

SCSI Controller

The used SCSI controller is a LSI53C1010. It supports two dual U2W LVD SCSI buses with a SCSI data transfer rate of up to 160 MByte/s for each channel. Both SCSI interfaces are available via the front panel.

Two interrupts are generated by the SCSI controller for interrupting the main processor.

Both SCSI interfaces have an on–board termination which can be enabled and disabled via on–board switches. By default, the SCSI termination is enabled.

SENTINEL64 PCI-to-PCI Bridge

The SENTINEL64 PCI–To–PCI bridge is used to connect the primary PCI bus A to the secondary PCI bus B. For details about the SENTINEL64

device refer to the SENTINEL64 Reference Guide available via the Force Computers S.M.A.R.T. server.

PCI-to-VME Bridge

The used PCI–To–VME bridge is a Tundra Universe II device. Its main features are:

- Fully compliant to VME64 bus standard
- Integral FIFOs for write posting to maximize bandwidth utilization
- Programmable DMA controller with linked–list mode
- CPU or peripheral boards functioning as both master and slave in the
- Sustained transfer rates up to 60–70 Mbytes/s

Note: When operating the board in system slot 1, the system clock is disabled while the board is in reset. This is a limitation of the Universe II device.

PCI Bus B

PCI bus B runs at 33 MHz and is 64 bit wide. It is the secondary PCI bus of the CPU board and has the following devices attached to it:

- Ethernet controller
- Southbridge
- PCIO–2 controller
- PMC module

Ethernet Controller

The Ethernet controller used at PCI bus B is the same as is used at PCI bus A.

Southbridge

The used Southbridge is an ALI M1535D+. It provides the following interfaces:

- Two IDE channels with ATA–100
- Parallel interface
- Floppy disk interface
- PS/2 keyboard/mouse interface
- SUN keyboard/mouse interface via two serial interfaces

PCIO-2 Controller

The used PCIO–2 controller is a SUN SME2300. It is a single–chip I/O subsystem using a single PCI load and providing the following interfaces:

- Expansion bus (EBus) interface
- Four USB interfaces
- Media Independent Interface (MII)

EBus Interface

The PCIO-2 controller acts as EBus controller of the attached EBus. A description of all devices attached to the EBus is given below.

Media Independent Interface

Two on-board Intel LXT971 PHY devices are connected to the MII. They transform the MII into a 10/100BaseT Ethernet interface which is available either via front panel or via IOBP.

Important features of the PHY device are:

- Support for ISO/IEC 8802-3 Ethernet
- Support for Shielded Twisted Pair (STP) and Unshielded Twisted Pair (UTP) category-5 cables of up to 100 meters length
- Operation in half-duplex and full-duplex mode possible
- Speed adjustion either manually or via auto-negotiation

USB Interfaces

Four USB channels are provided with each channel supporting 1.5 MBit/s and 12 MBit/s. All USB interfaces provide auto resume from power managed (suspended) state.

The USB interfaces 1, 2 and 3 are routed to the CPU board's IOBP where they are available via three front connectors. USB interface 4 is unused.

The USB interfaces provide the host controllers for USB transfers and a four-port integrated hub. The host controller manages the control and data flow. It also provides connection management and provides status information. The hub enables tiered star topology to provide multiple connections.

EBus

The EBus is a generic slave 8-bit wide Direct Memory Access (DMA) bus (pseudo ISA bus) to which the following devices are connected:

- Field-Programmable Gate Array (FPGA)
- PLCC PROM and flash memory device
- Real time clock and NVRAM
- Quad serial controller

FPGA

The used FPGA is a Spartan XCS20XL device made by XILINX. It provides the following main features:

- Watchdog
- Timer
- Temperature sensor control
- Two local I^2C interfaces
- Ethernet interface 1/3 switching
- LED and switch control
- Reset control

Watchdog

The CPU board's watchdog is implemented inside the FPGA. It is used to reset the board after a configured time, if no software trigger occurred. If enabled in the Interrupt Enable Control register, an interrupt will be generated before the watchdog timer runs out.

The watchdog can be enabled by setting SW1-3 to ON. It starts with the first trigger of the watchdog trigger bit in the Watchdog Trigger register. After the watchdog was started, it is not possible to stop it anymore.

The Watchdog Timer Control Register allows to specify the time after which an interrupt is generated and after which a reset is issued. For both, values between 125 ms up to 1 hour in 15 steps are possible. The value of each following step is increased by a factor of between 1.5 and 3.

To be compatible to the predecessor board SPARC/CPU-54, the time after which a reset is issued after a reset is set to 2.5 s and the time after which an interrupt is generated is set to 1.25s. Once the watchdog timer is running, it is only possible to reduce the watchdog run out time.

Timer

The FPGA contains two timers which can be used as two independent 16-bit count-down timers with a timer interval of 10 μs and a maximum run-out time of 655.35 ms. Two independent interrupts are possible which can be enabled or disabled with the Interrupt Enable Control register. One counter read-back register set is also available which shows the correct timer values.

Both timers can be combined to run as one 32-bit count-down timer with a timer interval of 10 μs and a total run-out time of 42949.67295 s (or 11 h, 55 min, 49 s and 672.95 ms). In this mode only one interrupt is possible.

The timer counts down from its initial value to zero in steps of 10 μs. The initial value can be set by software from 1 to 65535 in 16-bit mode or from 1 to 4294967295 in the 32-bit mode, which results in a timer period of 10 μs to 655.35 ms in the 16-bit mode or of 10 μs to 42949.67295s in the 32-bit mode. If the timer has reached zero, an interrupt is generated, if enabled, and the timer loads its initial value to count down again.

A detailed description of all registers related to the timers is given in the chapter "Maps and Registers".

Temperature Sensor Control

The on-board temperature sensor device MAX1617 measures the temperatures of the CPU board and the CPU. If the measured temperatures is not within a pre-defined range between lower and upper temperature, bit 2 is set in the External Failure Register and, if enabled, an interrupt is generated.

Local I2C Interface

Two separate I^2C buses are available on the CPU board. Both are implemented in the Xilinx FPGA and have the following devices attached to them:

- Serial Presence Detects (SPDs)
- On-board temperature sensor
- Board Information Blocks (BIBs)

BIBs are used for internal purposes only and are therefore not further described in this guide. All other devices are I2C bus slaves and are identified by unique addresses which are given in the table below.

Device	I2C Bus	I2C Bus Slave Address
Temperature sensor MAX1617	2	0011.000_2
SPD CPU–56 PROM Bank 1–4 24C04 Serial E^2PROM	2	$1010.00x_2$
SPD MEM–550 PROM Bank 1–4 24C04 Serial E^2PROM	2	$1010.01x_2$

Ethernet Interface 1/3 Switching

As mentioned earlier in this guide, Ethernet interface 1 is available via front panel and Ethernet interface 3 via the CPU board's IOBP. Only one of both interfaces can be active at the same time.

The selection which interface is active is made at board reset by the FPGA's internal logic. It depends on the Miscellaneous Control Register bits 5 to 7 and on which Ethernet interface provides a link. The Miscellaneous Control Register is set by OpenBoot while booting the board. For information on how to change the default setting, refer to the *SPARC/CPU–56(T) OpenBoot Enhancements Programmer's Guide* which is available via the Force Computers S.M.A.R.T. service.

By default, the selection is made as described in the following table.

Link at Interface 1	Link at Interface 3	Activated Ethernet Interface
Yes	Yes	1
Yes	No	1
No	Yes	3
No	No	1

LED and Switch Control

The FPGA internal logic is responsible for:

- Control of front panel LEDs
- Readback of switches SW1–4

Reset Control

The FPGA handles all resets and distributes them to the CPU. Possible reset sources are listed in the following table.

Table 12: *Reset Sources*

Reset Source	Description
Watchdog reset	On expiry, the watchdog timer can generate a reset.
Front panel key	Depending on the time the key is pressed, either a reset or a board abort is issued
Two-pin connector on CPU board's IOBP	By shortcutting this connector a reset is issued
VMEbus	Two directions are possible: the VMEbus resets the CPU board or the CPU board resets the VME bus
Power-up reset	If one or more on-board voltages are not within their thresholds, a reset is issued
PMC reset	A PMC module in non-monarch mode can reset the CPU board

PLCC PROM and Flash Memory Device

The following memory devices are connected to the EBus:

- One PLCC PROM with 1 MByte address space
- One flash memory device with 16 MByte address space

The PLCC PROM is the device from which the CPU board boots by default.

The 16 MByte flash memory device can be used as:

- User flash memory of 16 MBytes
- Boot flash memory of 1 MByte with the remaining 15 MBytes used as user flash memory

The selection between both operation modes is made via on-board switches.

Whether to boot from the PLCC PROM or the flash memory device, is determined by switch SW1-2. After booting, the whole PLCC PROM is switched off, regardless of the position of switch SW 1-2. Switch SW1-1 is used to enable write-protection of the flash memory device. If this switch is OFF (default), the flash memory device is write-protected. In order to copy the PLCC PROM content to the flash memory device, switch SW1-1 must be switched ON and switch SW1-2 must be set to OFF.

Real-T ime Clock and NVRAM

The CPU board provides the M48T35AV with an real–time clock (RTC) and a non–volatile RAM (NVRAM) which offers the following features:

- 32 KByte ultra–low power CMOS SRAM
- Byte–wide accessible real–time clock
- Long–life lithium carbon mono fluoride battery
- Year–2000 compliant RTC with own crystal

Serial Controller

The CPU board provides four independent full–duplex serial I/O interfaces. They are implemented via the Quad Enhanced Serial Communication Controller 16C554 by Texas Instruments.

The device offers the following features:

- Four independent full–duplex serial channels
- Four independent baud rate generators
- Hardware handshake support (RTS/CTS/DTR/DTS/RI/DCD)
- Interrupt controlled

Interface 1 and 2 are available on the front panel via two micro DSub connectors. The interfaces 3 and 4 are routed to the SPARC/IOBP–CPU–56 via the P2 connector.

5

OpenBoot Firmware

Introduction

The OpenBoot firmware consists of the Common Operations and Reset Environment (CORE), the power–on selftest (POST), the OpenBoot Diagnostics (OBDIAG), and the OpenBoot itself as well as support for the VxWorks real–time operating system (RTOS).

The OpenBoot firmware is subject to changes. For the newest version and how to upgrade, refer to the SMART service accessible via the Force Computers World Wide Web site (www.forcecomputers.com).

Note: The appearance of the on–screen output shown in the examples can differ from the appearance of the output on your monitor according to your device tree (CPU architecture).

For more information on the OpenBoot firmware, see the *OpenBoot 4.x Manual Set*.

CORE

CORE is responsible for setting up proper environments for booting purposes. It first initializes the system to a status where different firmware can be loaded from.

CORE automatically transfers control to its clients (such as OpenBoot, VxWorks, Chorus Booter...) during power up.

Furthermore, it provides a unified interface for using public CORE functions. Thus, the CORE unifies system initialization and minimizes modifications within the upper level firmware.

The following figure gives a system overview of which systems are initialized by CORE.

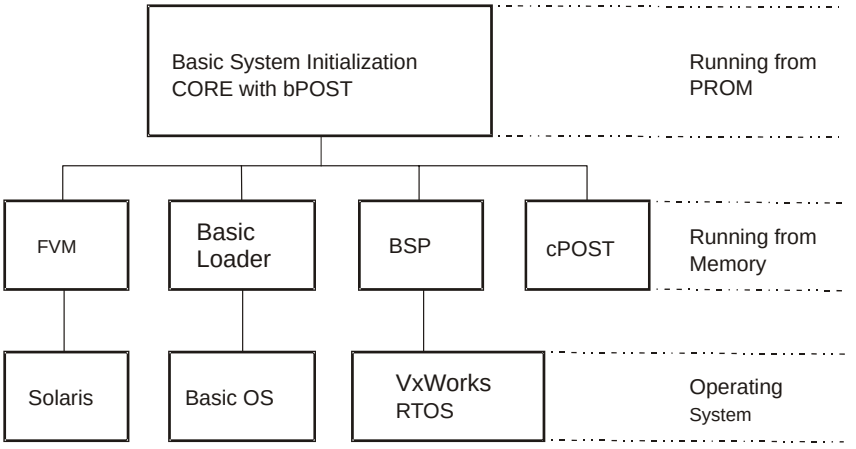


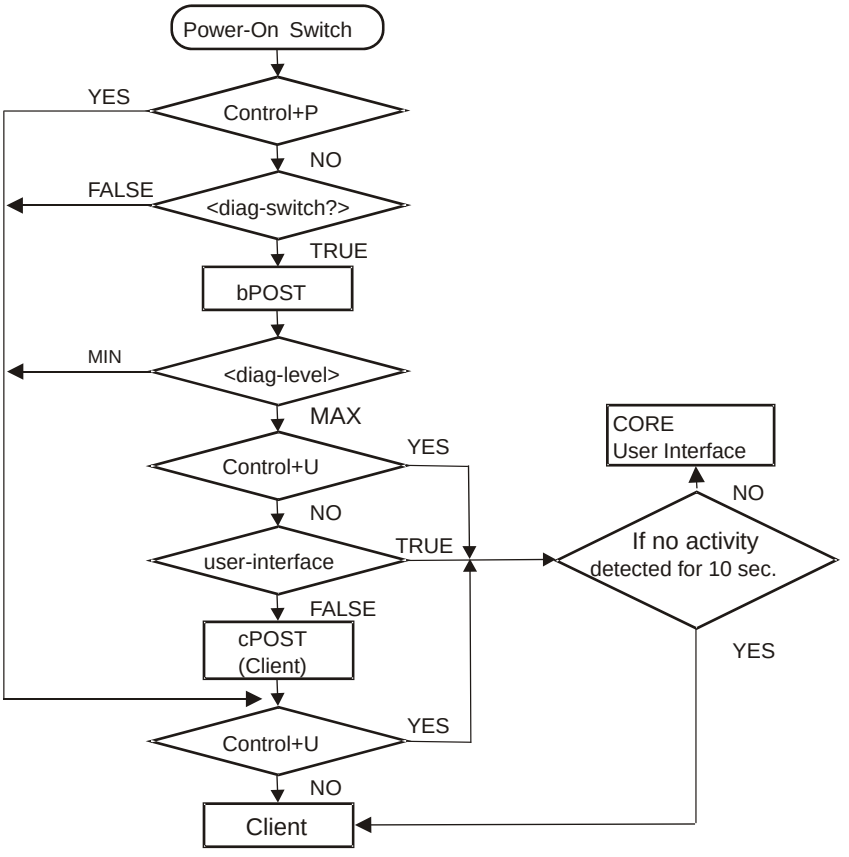
Figure 21: *OpenBoot CORE Overview*

Additionally, CORE is designed to reach the following goals:

- Ability to use I/O devices including serial port, flash, floppy, and net early on the cold boot sequence of a firmware client.
- Basic system tests that can replace existing POST in min. mode.
- System testing may be done using the POST drop–in in max. mode.
- Error recovery from exceptions which currently do not exist in OpenBoot and from any fatal conditions during flash update
- Developing standard validation test suites that could prevent major bugs in CORE and clients
- Sample client codes that could facilitate any client porting

CORE Workflow

The following figure describes the workflow of CORE.



CORE Commands

In order to change or interrupt the boot process in CORE, the following commands can be executed:

- Skip POST: <Control>+<P>
- Enter user interface: <Control>+<U>
- User default NVRAM variables for this run: <Control>+<N>
- Turn-on messages (if <diag-switch> is set to true): <Control>+<M>

POST

At hardware power-on or button power-on, the CORE firmware executes POST if the NVRAM configuration parameter <diag-switch?> was set to true beforehand. The extents of certain tests executed within in the POST depend on the state of the configuration parameter <diag-level>.

You choose between minimal or maximal testing by setting this configuration parameter to min or max. If the NVRAM configuration parameter <diag-switch?> is true for each test, a message is displayed on a terminal connected to the serial I/O interface A.

If the system does not work correctly, error messages will be displayed which indicate the problem. After POST, the OpenBoot firmware boots an operating system or enters the Forth monitor, if the NVRAM configuration parameter <auto-boot?> is false.

OpenBoot

Booting the system is the most important function of the OpenBoot firmware.

Booting is the process of loading and executing a stand-alone program such as the operating system. After the system is powered on, it usually boots automatically after it has passed POST which occurs without user intervention.

If necessary, you can explicitly initiate the boot process from the OpenBoot command prompt. Automatic booting uses the default boot device specified in the nonvolatile RAM (NVRAM). User-initiated booting either uses the default boot device or one specified by the user.

In order to boot the system from the default boot device with default settings, enter the following command at the Forth monitor prompt ok:

```
ok boot
```

The boot command has the following format:

boot <device-specifier> <filename> <-bootoption>

Optional Boot Parameters

Table 13: *Boot Parameters*

Parameter	Description
<device-specifier>	Name (full path or alias) of the boot device. Typical values are cdrom, disk, floppy, net or tape.
<filename>	Name of program to be booted The filename parameter is relative to the root of the selected device. If no filename is specified, the boot command uses the value of the boot file NVRAM parameter. The NVRAM parameters used for booting are described in the following section.
<-bootoption>	Bootoption may be one of the following: -a: Prompts interactively for device and name of boot file -h: Halts after loading program -r: Reconfigures Solaris device drivers after changing hardware configuration -v: Prints verbose information during boot procedure

Boot Devices

To explicitly boot from the internal disks using the Forth Monitor, enter:

```
ok boot disk
```

or

```
ok boot disk-2
```

To retrieve a list of all device alias definitions, enter at the Forth Monitor command prompt:

```
devalias
```

The following table lists device aliases available for SCSI devices.

Table 14: *OpenBoot Aliases for SCSI Devices*

Alias	SCSI Device	SCSI Interface
disk	Disk SCSI-target-ID 0	1
diskf	Disk SCSI-target-ID f	1
diske	Disk SCSI-target-ID e	1
diskd	Disk SCSI-target-ID d	1
diskc	Disk SCSI-target-ID c	1
diskb	Disk SCSI-target-ID b	1

Alias	SCSI Device	SCSI Interface
diska	Disk SCSI–target–ID a	1
disk9	Disk SCSI–target–ID 9	1
disk8	Disk SCSI–target–ID 8	1
disk7	Disk SCSI–target–ID 7	1
disk6	Disk SCSI–target–ID 6	1
disk5	Disk SCSI–target–ID 5	1
disk4	Disk SCSI–target–ID 4	1
disk3	Disk SCSI–target–ID 3	1
disk2	Disk SCSI–target–ID 2	1
disk1	Disk SCSI–target–ID 1	1
disk0	Disk SCSI–target–ID 0	1
tape (or tape0)	First tape drive SCSI–target–ID 4	1
tape1	Second tape drive SCSI–target–ID 5	1
cdrom	CD–ROM partition f, SCSI–target–ID 6	1
scsi–2	SCSI 2	2
disk–2	Default disk SCSI–target–ID 0	2
disk2f	Disk SCSI–target–ID f	2
disk2e	Disk SCSI–target–ID e	2
disk2d	Disk SCSI–target–ID d	2
disk2c	Disk SCSI–target–ID c	2
disk2b	Disk SCSI–target–ID b	2
disk2a	Disk SCSI–target–ID a	2
disk29	Disk SCSI–target–ID 9	2
disk28	Disk SCSI–target–ID 8	2
disk27	Disk SCSI–target–ID 7	2
disk26	Disk SCSI–target–ID 6	2
disk25	Disk SCSI–target–ID 5	2
disk24	Disk SCSI–target–ID 4	2

Alias	SCSI Device	SCSI Interface
disk23	Disk SCSI–target–ID 3	2
disk22	Disk SCSI–target–ID 2	2
disk21	Disk SCSI–target–ID 1	2
disk20	Disk SCSI–target–ID 0	2
tape–2 (or tape20)	First tape drive SCSI–target–ID 4	2
tape21	Second tape drive SCSI–target–ID 5	2
cdrom–2	CD–ROM partition f, SCSI–target–ID 6	2

The following table lists device aliases available for other devices.

Table 15: *OpenBoot Aliases for Miscellaneous Devices*

Alias	Device
cdrom–3	CD–ROM partition f, on–board IDE secondary master
disk–3	Disk, on–board IDE primary master
disk33	Disk, on–board IDE secondary slave
disk32	Disk, on–board IDE secondary master
disk31	Disk, on–board IDE primary slave
disk30	Disk, on–board IDE primary master
ide	on–board IDE
ebus	EBus
flash	Flash EPROM
flash–prog	Flash EPROM programming mode
floppy	Floppy disk
keyboard	Keyboard
mouse	Mouse
net	Ethernet 1 interface via front panel
net2	Ethernet interface 2
net3	Ethernet 3 interface via IOBP
pci	Primary PCI bus
ttya	Serial interface A

Alias	Device
ttyb	Serial interface B
tyyc	Serial interface C
tyyd	Serial interface D
vme	VME

OBDIAG

OBDIAG stands for OpenBoot Diagnostics and is an additional diagnostics drop–in driver program which serves as an NVRAM configuration feature.

It allows to test the hardware by calling OBDIAG when the OpenBoot firmware is present and the <ok> prompt has appeared. During the start–up sequence of the CPU, OpenBoot searches for the presence of devices on all expansion buses and evaluates their characteristics such as device ID, device type, vendor ID, and revision ID. In order to test the hardware, OBDIAG requires selftest methods for the discovered devices. If OBDIAG does not find any selftest methods in the device nodes, it looks for its own selftest methods.

Executing OBDIAG

There are two different methods to execute OBDIAG:

a) Via Script

b) Manually

Via Script

In order to execute OBDIAG via script, set two configuration variables by enterring:

```
setenv mfg-mode chamber
```

```
setenv diag-switch? true
```

Now a script of additional diagnostic tests is executed automatically after each POST from OBDIAG provided that POST has been running without failure during hardware power on.

Manually

In order to execute OBDIAG manually, enter the following command at the ok prompt:

```
obdiag
```

When OBDIAG is called, the <obdiag> test prompt appears and you can now choose the required test. You can run single tests, a number of tests, all tests, or all tests with exceptions. If the test has passed successfully, a short test comment will appear on screen. In order to return to the main menu, hit the enter key.

Terminating OBDIAG

In order to terminate OBDIAG and return to OpenBoot, enter

```
exit
```

The OpenBoot prompt will then reappear.

OBDIAG Commands

Apart from testing the hardware, you can also call several commands which can be seen in the ODBIAG main menu. The following table provides an overview of these commands.

Table 16: *OBDIAG Commands*

Command	Description
exit	Exits obdiag tool
help	Prints this help information
setenv	Sets diagnostic configuration variable to new value
printenvs	Prints values for diagnostic configuration variables
versions	Prints selftests, library, and obdiag tool versions
test–all	Tests all devices displayed in the main menu
test 1,2,5	Tests devices 1, 2, and 5
except 2,5	Tests all devices except for devices 2 and 5
what 1,2,5	Prints some selected properties for devices 1, 2, and 5

OBDIAG provides a brief excerpt of the OpenBoot configuration variables. The values of the variables are displayed after entering the following command:

```
printenvs
```

You can decide whether the chosen test will either stop at the occurrence of the first error or continue to test the hardware. It is also possible to run the test more than once or produce a detailed print–out of the test.

The example below shows the detailed print out of an OBDIAG test.

Example:

```
obdiag> setenv diag-verbosity 2
diag-verbosity = 2
Hit any key to return to the main menu <cr>
obdiag> setenv diag-continue? 0
diag-continue? = 0
Hit any key to return to the main menu <cr>
obdiag> test 2
Hit the spacebar to interrupt testing
Testing /pci@1f,0/ebus@1
SUBTEST: vendor-id-test
SUBTEST: device-id-test
SUBTEST: mixmode-read
SUBTEST: e2-class-test
SUBTEST: status-reg-walk1
SUBTEST: line-size-walk1
SUBTEST: latency-walk1
SUBTEST: line-walk1
SUBTEST: pin-test
SUBTEST: dma-reg-test
SUBTEST: dma-func-test
Selftest at /pci@1f,0/ebus@1 .....................................
passed
Hit any key to return to the main menu <cr>
obdiag> exit <cr>
ok
```

VxWorks Support

ThePLCC PROM delivered together with the CPU board contains support for the real–time operating system VxWorks 5.4 from WindRiver Systems. A VxWorks booter, “bootrom.hex” image, is provided as dropin named “bootrom”. In order to execute it, enter at the CORE command prompt;

```
execute bootrom
```

To automatically start the VxWorks booter at power up, enter:

```
set kernel bootrom
```

NVRAM Boot Parameters

The OpenBoot firmware holds its configuration parameters in NVRAM. To see a list of all available configuration parameters, enter at the Forth Monitor prompt: **`printenv`**

As you can see in the list, the default setting is for the CPU board to boot the operating system automatically. If this is not the case, ensure that the <auto-boot?> parameter is set to true.

To set specific parameters, use the setenv command as follows: **`setenv <configuration_parameter> <value>`**

The configuration parameters in the following table are involved in the boot process.

Table 17: *OpenBoot Configuration Parameters*

Parameter	Default Value	Description
auto-boot?	true	If true, automatic booting after power on or reset
boot-device	disk	Device from which to boot
boot-file	empty string	File to boot
diag-switch?	false	If true, run in diagnostic mode, test results are shown, boot up takes longer If false, normal mode, short boot up
diag-device	net	Device from which to boot in diagnostic mode
diag-file	empty string	File to boot in diagnostic mode

When booting an operating system or another stand-alone program, and neither a boot device nor a filename is supplied, the boot command of the Forth monitor takes the omitted values from the NVRAM configuration parameters. If the parameter <diag-switch?> is false, the parameters <boot-device> and <boot-file> are used. Otherwise, the OpenBoot firmware uses the parameters <diag-device> and <diag-file> for booting.

Diagnostics

The Forth Monitor includes several diagnostic routines. These on-board tests let you check devices such as network controller, SCSI devices, floppy disk system, memory, clock, keyboard and audio. User-installed devices can be tested if their firmware includes a self-test routine.

The table below lists several diagnostic routines.

Table 18: *Diagnostic Routines*

Command	Description
probe-scsi	Identifies devices connected to the on-board SCSI controller
probe-scsi-all [<device-path>]	Performs probe-SCSI on all SCSI controllers installed in the system below the specified device tree node. If <device-path> is omitted, the root node is used.
test [<device-specifier>]	Executes the specified device's self-test method. <device-specifier> may be a device path name or a device alias. Example: test net - test network connection
test-all [<device-specifier>]	Tests all devices that have a built-in self-test method and that reside below the specified device tree node. If <device-specifier> is omitted, the root node is used.
watch-clock	Monitors the clock function.
watch-net	Monitors network connection via primary Ethernet
probe-ide	Identifies devices connected to IDE bus
probe-ide-all [<device-path>]	Performs probe-ide on all IDE buses installed in the system below the specified device tree. If <device path> is omitted, the root node is used.

SCSI Bus

To check the on-board SCSI#1 or SCSI#2 for connected devices, enter:

```
ok probe-scsi
Primary UltraSCSI bus:
Target 1
 Unit 0 Disk WDIGTL WDE9100 ULTRA2 1.21
-
Secondary UltraSCSI bus:
```

```
-
ok
```

All SCSI Buses

To check all SCSI buses installed in the system, enter the following:

```
probe-scsi-all
```

The actual response depends on the devices on the SCSI buses.

Note: A terminal message as answer to the command probe–scsi–all can take up to two minutes.

```
ok probe-scsi-all
/pci@1f,0/scsi@2
Target 6
Unit 0 Disk Removable Read Only Device SONY CD-ROM CDU-8012 3.1a
/pci@1f/pci@4,1/scsi@2
Target 3
Unit 0 Disk FUJITSU M2952ESP SUN2.1G2545
ok
```

Single Device

To test a single installed device, enter:

```
test <device-specifier>
```

This executes the self–test device method of the specified device node.

Group of Devices

To test a group of installed devices, enter:

```
test-all
```

All devices below the root node of the device tree are tested. The response depends on the devices having a self–test method. If a device specifier option is supplied at the command line, all devices below the specified device tree node are tested.

Clock

To test the clock function enter:

```
ok watch-clock
Watching the ‘seconds’ register of the real time clock chip.
It should be ‘ticking’ once a second.
Type any key to stop.
22
ok
```

The system responds by incrementing a number every second. Press any key to stop the test.

Network

To monitor the network connection enter:

```
ok watch-net
Internal loopback test -- succeeded.
Transceiver check -- Using Onboard transceiver -- Link Up.
passed
Using Onboard transceiver -- Link Up.
Looking for Ethernet packets.
‘.’ is a good packet. ‘X’ is a bad packet.
Type any key to stop.
...........X.........................X.............
ok
```

The system monitors the network traffic. It displays a dot (.) each time it receives a valid packet and displays an X each time it receives a packet with an error which can be detected by the network hardware interface.

IDE Devices

The following is an example output obtained after enterring probe–ide.

```
ok probe-ide
 Device 0 ( Primary Master )
 Not Present
 Device 1 ( Primary Slave )
 Not Present
 Device 2 ( Secondary Master )
 Removable ATAPI Model: TOSHIBA CD-ROM XM-6702B
 Device 3 ( Secondary Slave )
 Not Present
ok
```

Displaying System Information

The Forth Monitor provides several commands to display system information such as the system banner, the Ethernet address for the Ethernet controller, the contents of the ID PROM, and the version number of the OpenBoot firmware.

Ethernet Address and Host ID

In order to see the Ethernet address and host ID, enter the following command at the OpenBoot prompt:

```
ok banner
```

The figures below explain how the CPU board's Ethernet address and the host ID are determined.

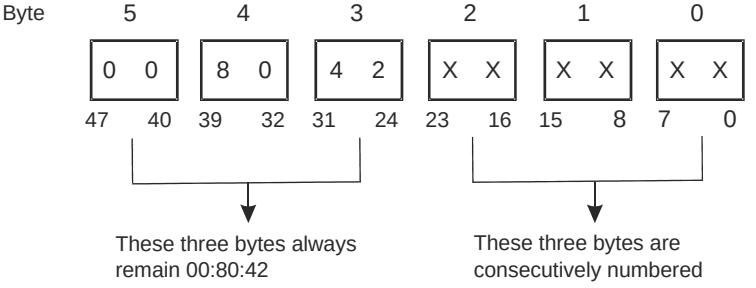


Figure 22: *48-bit (6-byte) Ethernet Address*

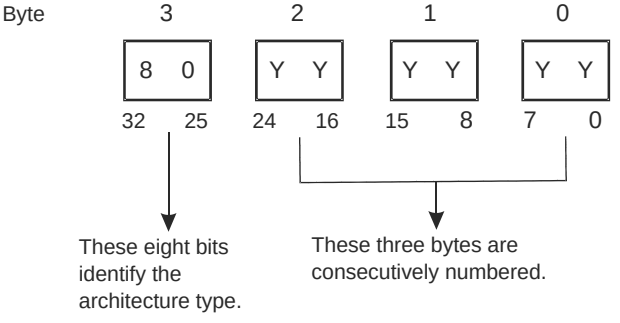


Figure 23: *32-bit (4-byte) Host ID*

ID PROM

The ID PROM contains specific information on the individual machine including the serial number, date of manufacture, and assigned Ethernet address. The following table lists these commands.

Table 19: *Commands to Display System Information*

Command	Description
banner	Displays system banner
.enet-addr	Displays the Ethernet address.
.idprom	Displays ID PROM contents, formatted
.traps	Displays a list of SPARC trap types
.version	Displays version and date of the boot PROM
show-devs	Displays a list of all device tree nodes
devalias	Displays a list of all device aliases

Resetting the System

If your system needs to be reset, there are two possibilities:

- Software reset
  For this type of reset, use the command reset at the Forth command line.
- Button power–on reset

In both cases the system begins with the initialization procedures. If the system is reset via a button power–on reset, the power–on self test is executed before the initialization if the NVRAM configuration variable <diag–switch?> is set true.

Activating OpenBoot Help

The Forth Monitor contains an online help which can be activated by entering the command help. Entering help creates the following screen output.

```
ok help
Enter ‘help command-name’ or ‘help category-name’ for more help
(Use ONLY the first word of a category description)
Examples: help select -or- help line
Main categories are:
Numeric output
Radix (number base conversions)
Arithmetic
Memory access
Line editor
System and boot configuration parameters
Select I/O devices
Floppy eject
Power-on reset
Diag (diagnostic routines)
Resume execution
File download and boot
Nvramrc (making new commands permanent)
ok
```

A list of all available help categories is displayed. These categories may also contain subcategories. To get help for special Forth words or subcategories, enter

```
help <name>
```

The online help shows you the Forth word, the parameter stack before and after execution of the Forth word (before –– after), and a short description.

The online help of the Forth monitor is located in the boot PROM. This means that an online help is not available for all Forth words.

Typical examples for how to get help for special Forth words or subcategories are given below.

```
ok help power
reset-all reset-machine, (simulates power cycling )
power-off Power Off
ok
ok help memory
dump ( addr length -- ) display memory at addr for length bytes
fill ( addr length byte -- ) fill memory starting at addr with
byte
move ( src dest length -- ) copy length bytes from src to dest
address
map? ( vaddr -- ) show memory map information for the virtual
address
```

```
x? ( addr -- ) display the 64-bit number from location addr
l? ( addr -- ) display the 32-bit number from location addr
w? ( addr -- ) display the 16-bit number from location addr
c? ( addr -- ) display the 8-bit number from location addr
x@ ( addr -- n ) place on the stack the 64-bit data at location
addr
l@ ( addr -- n ) place on the stack the 32-bit data at location
addr
w@ ( addr -- n ) place on the stack the 16-bit data at location
addr
c@ ( addr -- n ) place on the stack the 8-bit data at location
addr
x! ( n addr -- ) store the 64-bit value n at location addr
l! ( n addr -- ) store the 32-bit value n at location addr
w! ( n addr -- ) store the 16-bit value n at location addr
c! ( n addr -- ) store the 8-bit value n at location addr
ok
```

6

Maps and Registers

Interrupt Map

The following table lists all interrupt sources, their vectors from the UIC to the PIE, their vectors from the PIE to the processor's execution unit and the respective priority.

Interrupt Source	RIC Vector	CPU Internal Vector	Offset	Priority
VME ACFAIL#/SYSFAIL# rising edge	17_{16}	$7C8_{16}$	08_{16}	6
Audio	24_{16}	$7E3_{16}$	23_{16}	8
Ethernet interface 2	16_{16}	$7D8_{16}$	18_{16}	6
Ethernet interface 4	15_{16}	$7C2_{16}$	02_{16}	5
Floppy interface	29_{16}	$7E7_{16}$	27_{16}	8
IDE interface 1	$1F_{16}$	$7E4_{16}$	24_{16}	7
IDE interface 2	$1F_{16}$	$7E4_{16}$	24_{16}	7
Parallel interface	22_{16}	$7E2_{16}$	22_{16}	2
Ethernet interface 1/3	21_{16}	$7E1_{16}$	21_{16}	3
USB interface	$0F_{16}$	$7C4_{16}$	04_{16}	7
PMC1 A	39_{16}	$7CD_{16}$	$0D_{16}$	4
PMC1 B	03_{16}	$7D2_{16}$	12_{16}	3
PMC1 C	$0C_{16}$	$7D5_{16}$	15_{16}	4
PMC1 D	$0B_{16}$	$7D6_{16}$	16_{16}	3
PMC2 A	$1D_{16}$	$7C6_{16}$	06_{16}	5
PMC2 B	$1C_{16}$	$7DD_{16}$	$1D_{16}$	4
PMC2 C	$0C_{16}$	$7D5_{16}$	15_{16}	4
PMC2 D	$0B_{16}$	$7D6_{16}$	16_{16}	3
PMC3 A	28_{16}	$7E6_{16}$	26_{16}	7
PMC3 B	$1B_{16}$	$7DE_{16}$	$1E_{16}$	3
PMC3 C	$2A_{16}$	$7E8_{16}$	28_{16}	2
PMC3 D	$1A_{16}$	$7CF_{16}$	$0F_{16}$	1
PMC4 A	$0E_{16}$	$7D4_{16}$	14_{16}	6
PMC4 B	38_{16}	$7C9_{16}$	09_{16}	5
PMC4 C	19_{16}	$7DF_{16}$	$1F_{16}$	1

Interrupt Source	RIC Vector	CPU Internal Vector	Offset	Priority
PMC4 D	09_{16}	$7D7_{16}$	17_{16}	1
PS/2 keyboard	$2B_{16}$	$7E9_{16}$	29_{16}	4
PS/2 mouse	$2C_{16}$	$7EA_{16}$	$2A_{16}$	4
SCSI interface 1	20_{16}	$7E0_{16}$	20_{16}	3
SCSI interface 2	14_{16}	$7D9_{16}$	19_{16}	4
SCSI interface 3	$0D_{16}$	$7C5_{16}$	05_{16}	5
Serial interface 1	$2D_{16}$	$7EB_{16}$	$2B_{16}$	7
Serial interface 2	04_{16}	$7D1_{16}$	11_{16}	4
Serial interface 3	$0A_{16}$	$7C7_{16}$	07_{16}	2
Serial interface 4	01_{16}	$7D3_{16}$	13_{16}	1
SUN keyboard	10_{16}	$7CA_{16}$	$0A_{16}$	2
SUN mouse	07_{16}	$7C0_{16}$	00_{16}	7
Temperature sensor	11_{16}	$7DB_{16}$	$1B_{16}$	1
Timer 1/Timer 2	06_{16}	$7D0_{16}$	10_{16}	6
VME_N[0]	18_{16}	$7CC_{16}$	$0C_{16}$	6
VME_N[1]	$1E_{16}$	$7DC_{16}$	$1C_{16}$	6
VME_N[2]	05_{16}	$7C1_{16}$	01_{16}	5
VME_N[3]	13_{16}	$7DA_{16}$	$1A_{16}$	3
VME_N[4]	02_{16}	$7C3_{16}$	03_{16}	2
VME_N[5]	00_{16}	$7CE_{16}$	$0E_{16}$	2
VME_N[6]	12_{16}	$7CB_{16}$	$0B_{16}$	1
VME_N[7]	17_{16}	$7C8_{16}$	08_{16}	6
Watchdog timer	25_{16}	$7E5_{16}$	25_{16}	8

Physical Memory Map

The UltraSPARC–IIi+ has a 41–bit wide physical address range. This address range is divided into some specified areas for e.g. the main memory or the PCI bus.

Each area is subdivided into other areas, e.g. the main memory area is subdivided into the different memory module areas with the memory banks. Some areas are subdivided further down to one register with one byte, i.e. the System Control registers in the EBus area are byte–oriented.

The tables on the following pages describe the areas with the related address maps. If an address map is subdivided into other areas, a separate table is available below and a reference to this table can be found in the description column.

UltraSPARC-IIi+ Physical Address Memory Map

The main address map gives an overview of the whole address space of the UltraSPARC–IIi+ CPU. This address range is used for the main memory, and the PCI bus. Each defined address space is divided into subspaces which are described in the next sections.

Table 20: *UltraSPARC–IIi+ Main Address Map*

Physical Address Range PA<40..0>	Size	Description	Access
$000.0000.0000_{16}$– $001.FFFF.FFFF_{16}$	8 GByte	Main memory	Cacheable
$002.0000.0000_{16}$ – $007.FFFF.FFFF_{16}$		Reserved	Cacheable
$008.0000.0000_{16}$ – $1FB.FFFF.FFFF_{16}$		Reserved	Noncacheable
$1FC.0000.0000_{16}$ – $1FD.FFFF.FFFF_{16}$	8 GByte	Reserved, do not use	Noncacheable
$1FE.0000.0000_{16}$ – $1FF.FFFF.FFFF_{16}$	8 GByte	PCI bus, processor subsystem, memory, clock control, and ECU	Noncacheable

Memory Address Map

The main memory address range is divided between on–board memory and the MEM–550 memory modules. Two banks of 256 MByte and four banks of 256 MByte result in a total amount of up to 2 GB main memory.

Table 21: *Main Memory Address Map*

Physical Address Range PA<41..0>	Size	Bank	Memory Location	DIMM Type
$000.0000.0000_{16}$ – $000.0FFF.FFFF_{16}$	256 MByte	0	On-board memory	DIMM 0
$000.8000.0000_{16}$ – $000.8FFF.FFFF_{16}$	256 MByte	2		DIMM 1
$001.0000.0000_{16}$ – $001.0FFF.FFFF_{16}$	256 MByte	4	SPARC/MEM-550	DIMM 2
$001.1000.0000_{16}$ – $001.1FFF.FFFF_{16}$	256 MByte	5		
$001.8000.0000_{16}$– $001.8FFF.FFFF_{16}$	256 MByte	6		DIMM 3
$001.9000.0000_{16}$– $001.9FFF.FFFF_{16}$	256 MByte	7		

UltraSPARC-IIi+ Internal CSR Space

The UltraSPARC–IIi+ internal configuration space registers (CSR) are used for the configuration of the peripheral parts of the CPU, e.g. the PCI bus module (PBM), the I/O memory management unit (IOM), and the interrupt unit.

Table 22: *UltraSPARC–IIi+ Internal CSR Space*

Physical Address Range	Size	Description
$1FE.0000.0000_{16}$ – $1FE.0000.01FF_{16}$	512 Byte	PBM
$1FE.0000.0200_{16}$ – $1FE.0000.03FF_{16}$	512 Byte	IOM
$1FE.0000.0400_{16}$ – $1FE.0000.1FFF_{16}$	7 KByte	PCI interrupt engine (PIE)
$1FE.0000.2000_{16}$ – $1FE.0000.5FFF_{16}$	16 KByte	PBM
$1FE.0000.6000_{16}$ – $1FE.0000.9FFF_{16}$	12 KByte	PIE
$1FE.0000.A000_{16}$ – $1FE.0000.A7FF_{16}$	2 KByte	IOM
$1FE.0000.A800_{16}$ – $1FE.0000.EFFF_{16}$	22 KByte	PIE
$1FE.0000.F000_{16}$ – $1FE.00FF.F018_{16}$	23 MByte	Memory control unit (MCU)

Physical Address Range	Size	Description
$1FE.00FF.F020_{16}$	8 Byte	PIE
$1FE.00FF.F028_{16}$ – $1FE.00FF.FFFF_{16}$	4 KByte	MCU
$1FE.0100.0000_{16}$ – $1FE.0100.0041_{16}$	65 Byte	PBM

PCI Bus Address Map

The PCI bus address space is divided into areas for the different PCI accesses, e.g. configuration access, I/O access or memory access. These areas are distributed to the PCI devices on the SPARC/CPU-56.

The address allocation of the devices is made dynamically during the PCI configuration cycles after reset in OpenBoot. The allocation depends on the availibility of PCI devices (I/O board, PMC module).

The PCI device PCIO, part of the UltraSPARC–IIi+ chip set, must be available at power up for booting and has a fixed PCI address space. It has an interface to the EBus, where the boot PROM is located. Additionally, it has an interface to the MII bus from where the twisted–pair Ethernet interfaces are generated.

Table 23: *PCI Bus Address Map*

Address Range in PA<40:0>	Size	Description
$1FE.0100.0100_{16}$– $1FE.01FF.FFFF_{16}$	24 MByte – 256 Byte	PCI bus configuration space
$1FE.0200.0000_{16}$– $1FE.02FF.FFFF_{16}$	24 MByte	PCI bus I/O space
$1FE.0300.0000_{16}$– $1FE.FFFF.FFFF_{16}$	4 GByte – 48 MByte	Reserved
$1FF.0000.0000_{16}$– $1FF.FFFF.FFFF_{16}$	4 GByte	PCI bus memory space
$1FF.F000.0000_{16}$– $1FF.F17F.FFFF_{16}$	24 MByte	PCI bus memory space for the PCIO–2
$1FF.F180.0000_{16}$– $1FF.FFFF.FFFF_{16}$	256 MByte – 24 MByte	PCI bus memory space

PCIO-2 Address Map

The PCIO–2 has an address space of 24 MByte in total. It is divided into:

- 16 MByte for the boot PROM or flash memory on the EBus (CS0#)

- Seven address spaces for other EBus devices (CS1# – CS7#), e.g. RTC/NVRAM, the System Configuration registers or a serial controller.
- The PCIO–2 System Configuration registers

The detailed memory map is given in the following table. Memory areas which are not covered in the table are reserved for the EBus.

Table 24: *PCIO–2 Address Map*

Address Range in PA<40:0>	Size	EBus CS#	Description
$1FF.F000.0000_{16}$ – $1FF.F00F.FFFF_{16}$	1 MByte	0	PLCC PROM on the EBus (if SW1–1 is OFF and if bit 0 of the Miscellaneous Control register is set to 0)
$1FF.F010.0000_{16}$ – $1FF.F0FF.FFFF_{16}$	15 MByte	0	Reserved for the EBus (if SW1–1 is OFF and if bit 0 of the Miscellaneous Control register is set to 0)
$1FF.F000.0000_{16}$ – $1FF.F00F.FFFF_{16}$	1 MByte	0	Boot section of flash memory on the EBus (if SW1–1 is ON or if bit 0 of the Miscellaneous Control register is set to 1)
$1FF.F010.0000_{16}$ – $1FF.F0FF.FFFF_{16}$	15 MByte	0	User flash memory on the EBus (if SW1–1 is ON or if bit 0 of the Miscellaneous Control register is set to 1)
$1FF.F100.6000_{16}$ – $1FF.F100.7FFF_{16}$	8 KByte	1	RTC/NVRAM on the EBus
$1FF.F110.0000_{16}$ – $1FF.F11F.FFFF_{16}$	1 MByte	2	PLCC PROM mirror area (independent of SW2–1 and bit 0 of the Miscellaneous Control register)
$1FF.F130.0100_{16}$ – $1FF.F130.0108_{16}$	8 Byte	4	Serial controller on the EBus Serial interface A
$1FF.F130.0200_{16}$ – $1FF.F130.0208_{16}$	8 Byte	4	Serial controller on the EBus Serial interface B
$1FF.F130.0300_{16}$ – $1FF.F130.0308_{16}$	8 Byte	4	Serial controller on the EBus Serial interface C
$1FF.F130.0400_{16}$ – $1FF.F130.0408_{16}$	8 Byte	4	Serial controller on the EBus Serial interface D

Address Range in PA<40:0>	Size	EBus CS#	Description
$1FF.F160.0100_{16}$ – $1FF.F160.01FF_{16}$	256 Byte	7	System Configuration register on the EBus
$1FF.F170.0000_{16}$ – $1FF.F17F.FFFF_{16}$	1 MByte	n.a.	PCIO configuration registers

System Configuration Registers

The CPU board implements a set of system configuration registers via the field–programmable gate array (FPGA), which is accessible via the EBus.

The CPU Board System Configuration registers are used to control the on–board functions and to receive status information of the board. It is subdivided into 16 areas with 16 Bytes, each provided with a special function or reserved for future use.

In the following an overview of the System Configuration registers in the CPU board address space is given. Every register is described separately in the following chapters.

Overview of System Configuration Registers

The table below shows an overview of all registers in the CPU board address space.

Table 25: *CPU Board System Configuration Register Address Map*

Address Range in PA<40:0>	Size	Access	Default	Description
$1FF.F160.0100_{16}$	16 Byte			**Function Unit Miscellaneous Control**
$1FF.F160.0100_{16}$	1 Byte	r/w	00_{16}	Miscellaneous Control register
$1FF.F160.0110_{16}$	16 Byte			**Function Unit Display**
$1FF.F160.0110_{16}$	1 Byte	r/w	00_{16}	LED 1 Control register
$1FF.F160.0111_{16}$	1 Byte	r/w	00_{16}	LED 2 Control register
$1FF.F160.0112_{16}$	1 Byte	r/w	00_{16}	LED 3 Control register
$1FF.F160.0113_{16}$	1 Byte	r/w	00_{16}	LED 4 Control register
$1FF.F160.0120_{16}$	16 Byte			**Function Unit External Failure**
$1FF.F160.0120_{16}$	1 Byte	r	00_{16}	External Failure Status register
$1FF.F160.0130_{16}$	16 Byte			**Function Unit Watchdog**
$1FF.F160.0130_{16}$	1 Byte	r/w	08_{16}	Watchdog Control register
$1FF.F160.0131_{16}$	1 Byte	w	FF_{16}	Watchdog Trigger register
$1FF.F160.0134_{16}$	1 Byte	r	00_{16}	Watchdog Status register
$1FF.F160.0140_{16}$	16 Byte			**Function Unit Timer**

Address Range in PA<40:0>	Size	Access	Default	Description
$1FF.F160.0140_{16}$	1 Byte	r/w	00_{16}	Timer Control register
$1FF.F160.0141_{16}$	1 Byte	w	FF_{16}	Timer Clear Control register
$1FF.F160.0144_{16}$	1 Byte	r	00_{16}	Timer Status register
$1FF.F160.0148_{16}$	1 Byte	r/w	00_{16}	Timer 1 Init Control register U
$1FF.F160.0149_{16}$	1 Byte	r/w	00_{16}	Timer 1 Init Control register L
$1FF.F160.014A_{16}$	1 Byte	r/w	00_{16}	Timer 2 Init Control register U
$1FF.F160.014B_{16}$	1 Byte	r/w	00_{16}	Timer 2 Init Control register L
$1FF.F160.014C_{16}$	1 Byte	r	00_{16}	Timer 1 Counter Status register U
$1FF.F160.014D_{16}$	1 Byte	r	00_{16}	Timer 1 Counter Status register L
$1FF.F160.014E_{16}$	1 Byte	r	00_{16}	Timer 2 Counter Status register U
$1FF.F160.014F_{16}$	1 Byte	r	00_{16}	Timer 2 Counter Status register L
$1FF.F160.0180_{16}$	16 Byte			**Function Unit Interrupt**
$1FF.F160.0180_{16}$	1 Byte	r/w	00_{16}	Interrupt Enable Control register
$1FF.F160.0184_{16}$	1 Byte	r/w	00_{16}	Interrupt Pending Status register
$1FF.F160.01D0_{16}$	16 Byte			**Function Unit Reset**
$1FF.F160.01D4_{16}$	1 Byte	r	00_{16}	Reset Status register
$1FF.F160.01E0_{16}$	16 Byte			**Function Unit Board Status**
$1FF.F160.01E0_{16}$	1 Byte	r	FF_{16}	Switch 1 and 2 Status register
$1FF.F160.01E1_{16}$	1 Byte	r	FF_{16}	Switch 3 and 4 Status register
$1FF.F160.01E2_{16}$	1 Byte	r	00_{16}	Board Configuration 1 Status register
$1FF.F160.01E3_{16}$	1 Byte	r	00_{16}	Board Configuration 2 Status register
$1FF.F160.01EF_{16}$	1 Byte	r	00_{16}	Hardware Revision Status register
$1FF.F160.01F0_{16}$	16 Byte			**Function Unit I2C register**

Address Range in PA<40:0>	Size	Access	Default	Description
$1FF.F160.01FE_{16}$	1 Byte	r/w	00_{16}	I2C register 1
$1FF.F160.01FF_{16}$	1 Byte	r/w	00_{16}	I2C register 2

Miscellaneous Control Register

The Miscellaneous Control register is used to switch between the PLCC Boot PROM and the flash memory and to select availability of Ethernet interface 1.

Address: $1FF.F160.0100_{16}$

Table 26: *Miscellaneous Control Register*

Bit	Name	Description	Default	Access
0	TSOP EN	Used to switch between PLCC PROM access and flash memory access in the address space for CS0#. After reset, this bit is cleared (0). 0: If SW1–2 is OFF, the PLCC PROM is available in the CS0# address space. If SW1–2 is ON the flash memory is available in the CS0# address space. 1: The flash memory is available in the CS0# address space. **Note**: You can only write a ″1″ to this bit. After doing so, it can not be cleared anymore to ″0″.	0_2	r/w
1	PS/2 BACK	Used to switch between a rear connected and a front connected PS/2 keyboard/mouse. 0: Front panel PS/2 keyboard/mouse is enabled. 1: Rear panel PS/2 keyboard/mouse is enabled.	0_2	r/w
2	SER2_RS422EN	Used to enable the voltage supply for the RS–422 cable connected to the serial B interface. 0: Voltage supply is disabled. The ring indicator of the serial B interface can be used. 1: Voltage supply is enabled. The ring indicator of the serial interface B cannot be used.	0_2	r/w
3..4	–	These bits are always zero.	0_2	r

Bit	Name	Description	Default	Access
5..7	ETH1/3CTRL	These bits determine whether Ethernet interface 1 at the front panel or Ethernet interface 3 via IOBP is active. The selection is made by OpenBoot or VxWorks at board start-up. Per default, the selection is done automatically and depends on which Ethernet interface has a link. If both or no interfaces have a link, Ethernet interface 1 is preferred 000_2: No change of current status $0x1_2$: Ethernet interface 1 is enabled 010_2: Ethernet interface 3 is enabled $1x1_2$: Selection is made automatically with preference of interface 1 110_2: Selection is made automatically with preference of interface 3 **Note**: You can only write a ″1″ to each of these bits. After doing so, the respective bit can not be cleared anymore to ″0″.	–	w
5	ETH1 EN	Status of Ethernet interface 1 0: Disabled 1: Enabled	1_2	r
6	ETH3 EN	Status of Ethernet interface 3 0: Disabled 1: Enabled	0_2	r
7	Reserved	Always zero	0_2	r

User LED Control Registers

The following registers control front panel LED related features.

LED Control Register 1

This register is used to switch between the different operation modes of LED 1.

Address: $1FF.F160.0110_{16}$

Table 27: *LED Control Register 1*

Bit	Name	Description	Default	Access
4..0	LED_DISPLAY	Board status 00000_2: Red: Board reset Weak red: Board abort (during reset access) Green: Board running Blinking red/weak red: No PCI activity within the last two seconds Blinking green: No boot code found Weak red: 12V power supply on the VME backplane is not available User LED mode 00100_2: LED is OFF 00001_2: LED shines green 00010_2 : LED shines red IDE activity 10011_2: IDE 1/2 Ethernet activity 11000_2: Ethernet 1 11001_2: Ethernet 2 11010_2: Ethernet 3 11011_2: Ethernet 4 11100_2: Ethernet 1/3 11101_2: Ethernet 2/4 11111_2: Ethernet 1/2/3/4 At all other values, the LED is OFF.	00000_2	r/w
7..5		These bits are always zero		r

LED Control Register 2

This register is used to switch between the different operation modes of LED 2.

Address: 1FF.F160.0110$_{16}$

Table 28: *LED Control Register 2*

Bit	Name	Description	Default	Access
4..0	LED_DISPLAY	User LED mode 00000_2: OFF 00001_2 : Green 00010_2 : Red 00011_2 : Weak red 00101_2 : Slow blinking green (1/2 Hz) 00110_2 : Slow blinking red 00111_2 : Slow blinking weak red 01001_2 : Blinking green (1 Hz) 01010_2 : Blinking red 01011_2 : Blinking weak red 01101_2 : Fast blinking green (2 Hz) 01110_2 : Fast blinking red 01111_2 : Fast blinking weak red IDE activity 10011_2: IDE 1/2 Ethernet activity 11000_2: Ethernet 1 11001_2: Ethernet 2 11010_2: Ethernet 3 11011_2: Ethernet 4 11100_2: Ethernet 1/3 11101_2: Ethernet 2/4 11111_2: Ethernet 1/2/3/4 At all other values, the LED is OFF.	00000_2	r/w
7..5	Reserved	These bits are always zero.		r

LED Control Register 3

This register is used to switch between the different operation modes of LED 3.

Address: 1FF.F160.0112$_{16}$

Table 29: *LED Control Register 3*

Bit	Name	Description	Default	Access
4..0	LED_DISPLAY	VME activity 00000_2: Red: Universe II asserted VME SYSFAIL signal to the VMEbus. Green: Universe II accesses the VMEbus as master OFF: No VME SYSFAIL asserted and no activity of Universe User LED mode 00100_2: OFF 00001_2: Green 00010_2: Red Ethernet activity 11000_2: Ethernet 1 11001_2: Ethernet 2 11010_2: Ethernet 3 11011_2: Ethernet 4 11100_2: Ethernet 1/3 11101_2: Ethernet 2/4 11111_2: Ethernet 1/2/3/4 At all other values, the LED is OFF.	00000_2	r/w
7..5	Reserved	These bits are always zero.	r	

LED Control Register 4

This register is used to switch between the different operation modes of LED 4.

Address: 1FF.F160.0113$_{16}$

Table 30: *LED Control Register 4*

Bit	Name	Description	Default	Access
4..0	LED_DISPLAY	User LED mode 00000_2: OFF 00001_2 : Green 00010_2 : Red 00011_2 : Weak red 00101_2 : Slow blinking green (1/2 Hz) 00110_2 : Slow blinking red 00111_2 : Slow blinking weak red 01001_2 : Blinking green (1 Hz) 01010_2 : Blinking red 01011_2 : Blinking weak red 01101_2 : Fast blinking green (2 Hz) 01110_2 : Fast blinking red 01111_2 : Fast blinking weak red Ethernet activity 11000_2: Ethernet 1 11001_2: Ethernet 2 11010_2: Ethernet 3 11011_2: Ethernet 4 11100_2: Ethernet 1/3 11101_2: Ethernet 2/4 11111_2: Ethernet 1/2/3/4 At all other values, the LED is OFF.	00000_2	r/w
7..5		These bits are always zero.		r

External Failure Status Register

The External Failure Status register is used to receive information of external failure conditions: Overheating or power supply problems. All failure conditions can also be configured as an interrupt (refer to “Interrupt Registers” section).

Address: $1FF.F160.0120_{16}$

Table 31: *External Failure Register*

Bit	Name	Description	Default	Access
1..0	0	Reserved	00_2	r
2	TEMP_STAT	This bit reflects the state of the temperature sensor output. 0 : The temperature sensor did not detect a temperature outside of the specified range. 1: The temperature sensor has detected a temperature outside of the specified range.	0_2	r
5..3	0	Reserved	000_2	r
6	STAT ACFAIL	This bit reflects the state of the VMEbus low active ACFAIL signal, i.e. whether a failure of the power supply occurred. 0: The ACFAIL# signal is inactive (high). 1: The ACFAIL# signal is active (low).	0_2	r
7	STAT SYSFAIL	This bit reflects the state of the VMEbus low active SYSFAIL signal, i.e. whether a failure of the power supply occurred. 0: The SYSFAIL# signal is inactive (high). 1: The SYSFAIL# signal is active (low).	0_2	r

Watchdog Timer Registers

The watchdog timer is used to reset the board after a defined time interval, if no software trigger occurred. Before the watchdog timer runs out, an interrupt will be generated if it is enabled in the Interrupt Enable Control register. To enable the watchdog, switch SW1–3 must be set to ON. For details, refer to section "" on page NO TAG .

The watchdog starts with the first trigger of the watchdog trigger bit in the Watchdog Trigger register. After the watchdog is enabled, it is not possible to stop the watchdog. The watchdog timer can be configured to reset the board after a certain time interval which can vary between 125 ms and 1 hour. After reset, the time is set to 2.5 s for the reset and to 1.25 s for the interrupt, which is compatible to the SPARC/CPU–54.

Watchdog Timer Control Register

The Watchdog Timer Control register is used to set the time–out for the watchdog timer.

Note: If the watchdog is running, you can only change the watchdog time to a smaller value.

Address: 1FF.F160.0130$_{16}$

Table 32: *Watchdog Timer Control Register*

Bit	Name	Description	Default	Access
4..0	WDOG LENGTH	These bits are used to set the time–out for the watchdog timer. The tolerance of the time delay is 100ppm or +10 ms/–10 ms whichever is greater. The values given below indicate: Time after which reset is initiated/Time after which interrupt is triggered 00000_2: 125 ms/62 ms 00010_2: 250 ms/125 ms 00100_2: 500 ms/250ms 00110_2: 1 s/500 ms 01000_2: 2.5 s/1.25ms 01010_2: 5s/3 s 01100_2: 10 s/8 s 01110_2: 30 s/25 s 10000_2: 1 min/50 s 10010_2: 3 min/2 min 10100_2: 5 min/4 min 10110_2: 10 min/8 min 11000_2: 20 min/18 min 11010_2: 30 min/25 min 11100_2: 60 min/50 min 11111_2: Watchdog timer off	01000_2	r/w
7..5		These bits are always zero.		

Watchdog Timer Trigger Register

The Watchdog Timer Trigger register is used to trigger the watchdog timer.

Address: 1FF.F160.0131$_{16}$

Table 33: *Watchdog Timer Trigger Register*

Bit	Name	Description	Access
2..0	1	Reserved	w
3	WDOG TRIG	This bit is used to trigger the watchdog timer. If the watchdog is enabled through the switch SW1-3, the software must set this bit within the time period configured in the Watchdog Control register. If a watchdog interrupt is pending, it will be cleared by triggering the watchdog. 0: The watchdog timer is not triggered. 1: The watchdog timer is triggered.	w
7..4	1	Reserved	w

Watchdog Timer Status Register

The Watchdog Timer Status register reflects the watchdog timer status.

Address: 1FF.F160.0134$_{16}$

Table 34: *Watchdog Timer Status Register*

Bit	Name	Description	Default	Access
0	STAT WDOG	This bit reflects the status of the watchdog timer. 0: The watchdog timer has not reached the interrupt time. 1: The watchdog timer has exceeded the interrupt time. It is necessary to trigger the watchdog timer.	0_2	r
7..1	0	Reserved	0000000_2	r

Timer Registers

The timer can be used as two independent 16-bit countdown timers with a timer interval of 10 μs and a total maximum run-out time of 655.35 ms. Two independent interrupts are possible, which can be enabled or disabled (refer to "Interrupt Registers" section). A counter read-back register set is also available which always shows the correct timer value.

Both timers can also be used as one 32-bit countdown timer with a timer interval of 10 μs and a total run-out time of 42949.67295 s or 11h, 55min, 49 s and 672.95 ms. In this mode only one interrupt is available and possible.

The timer counts down from its initial value to zero in intervals of 10 μs. The initial value can be set by software from 1 to 65535 in the 16–bit mode or to 4294967295 in the 32–bit mode, which results in a timer period of 10 μs to 655.35 ms in 16–bit mode or 42949.67295 s in 32–bit mode. If the timer has reached zero, an interrupt is generated, if enabled, and the timer loads his initial value to count down again.

The timer has eleven registers in total. The first register is used to control the timer mode, one register is used to clear timer overruns, one register is used to read the timer overrun status, four registers are used for setting the initial timer values and the last four registers are used to read the current value of the countdown timers.

Timer Control Register

This register is used to set up the timer. If the timer is set to zero, the timer is off and no interrupts are generated. However, the Timer Status register will not be cleared. The normal timer tolerance is 100 ppm. During the first countdown after the timer activation, however, the timer tolerance is increased to 10 μs.

Address: $1FF.F160.0140_{16}$

Table 35: *Timer Control Register*

Bit	Name	Description	Default	Access
0	EN TIM1	Controls timer 1 0: Timer disabled 1: Timer enabled	0_2	r/w
1	EN MOD32	Switches between two 16–bit–wide timers and one 32–bit–wide timer 0: 16–bit mode enabled 1: 32–bit mode enabled	0_2	r/w
2..3	–	Reserved	00_2	r
4	EN TIM2	Controls timer 2 0: Timer disabled 1: Timer enabled	0_2	r/w
7..5	–	Reserved	000_2	r

Timer Clear Control Register

This register is used to control the status bits of both timers in the Timer Status register.

Address: 1FF.F160.0141$_{16}$

Table 36: *Timer Clear Control Register*

Bit	Name	Description	Access
0	CLR TIM1	Clears the status bits of timer 1 in the Timer Status register 0: Timer 1 status bits stay as they are. 1: Timer 1 status bits will be cleared.	w
3..1	–	Reserved	w
4	CLR TIM2	Clears the status bits of timer 2 in the Timer Status register 0: Timer 2 status bits stay as they are. 1: Timer 2 status bits will be cleared.	w
7..5	–	Reserved	w

Timer Status Register

The Timer Status register is used to recognize timer underrun conditions.

Address: 1FF.F160.0144$_{16}$

Table 37: *Timer Status Register*

Bit	Name	Description	Default	Access
0	STAT TIM1	Indicates an underrun of timer 1. This can only occur if timer 1 is enabled and the initial value is greater than 0. 0: No underrun of timer 1 has occurred. 1: An underrun of timer 1 has occurred.	0_2	r
1	ERR TIM1	Indicates that more than one timer underruns without clearance have occurred. It is a status for a missed timer underrun and can only occur if timer 1 is enabled and the initial value is greater than 0. 0: No more than one timer underruns of timer 1 have occurred. 1: More than one timer underruns of timer 1 have occurred.	0_2	r
2..3	–	Reserved	00_2	r
4	STAT TIM2	Indicates an underrun of timer 2. This can only occur if timer 2 is enabled, the initial value is greater than 0 and if the 16-bit mode is enabled. 0: No underrun of timer 2 has occurred. 1: An underrun of timer 2 has occurred.	0_2	r

Bit	Name	Description	Default	Access
5	ERR TIM2	Indicates that more than one timer underruns without clearance have occurred. It is a status for a missed timer underrun and can only occur, if timer 2 is enabled, the initial value is greater than 0 and if the 16-bit mode is enabled. 0: No more than one timer underruns of timer 2 have occurred. 1: More than one time underrun of timer 2 has occurred.	0_2	r
6..7	Reserved	Reserved	00_2	r

Timer Initial Control Registers

The following four registers are used to set up the run-out time of both timers. The 32 bits are distributed as big endian, which means the first register (1FF.F160.0148) represents the bits 31..24 and so on.

Address: $1FF.F160.0148_{16}$ - $1FF.F160.014B_{16}$

Table 38: *Timer Initial Control Registers*

Bit	Name	Description	Default	Access
15..0	TIMER2 INIT	Initialization time of timer 2 in 16-bit mode 0000_{16}: Timer disabled 0001_{16}: Timer run-out time is 10 μs $FFFF_{16}$: Timer run-out time is 655.35 ms	0000_{16}	r/w
31..16	TIMER1 INIT	Initialization time of timer 1 in 16-bit mode 0000_{16}: Timer disabled 0001_{16}: Timer run-out time is 10 μs $FFFF_{16}$: Timer run-out time is 655.35 ms	0000_{16}	r/w
31..0	TIMER1 INIT	Initialization time of timer 1 in 32-bit mode 0000.0000_{16}: Timer disabled 0000.0001_{16}: Timer run-out time is 10 μs $FFFF.FFFF_{16}$: Timer run-out time is 42949.67295 s	00000000_{16}	r/w

Timer Counter Status Register

The following four registers are used to read the current timer value of both timers. The 32 bits are also distributed as big endian. To obtain the correct timer status when reading all two or four bytes of a timer, an 16- or 32-bit access is necessary.

Address: 1FF.F160.014C$_{16}$ - 1FF.F160.014F$_{16}$

Table 39: *Timer Counter Status Register*

Bit	Name	Description	Default	Access
15..0	TIMER2 VALUE	Current value of timer 2 in 16-bit mode 0000_{16}: Timer 2 is not running. 0001_{16}: Timer 2 will initialize again during the next 10 μs. $7FFF_{16}$: Timer 2 needs 327.67 ms until next initialization. $FFFF_{16}$: Timer 2 needs 655.35 ms until next initialization.	0000_{16}	r
31..16	TIMER1 VALUE	Current value of timer 1 in 16-bit mode 0000_{16}: Timer 1 is not running. 0001_{16}: Timer 1 will initialize again during the next 10 μs. $7FFF_{16}$: Timer 1 needs 327.67 ms until next initialization. $FFFF_{16}$: Timer 1 needs 655.35 ms until next initialization.	0000_{16}	r
31..0	TIMER1 VALUE	Current value of timer 1 in 32-bit mode 0000.0000_{16}: Timer 1 is not running. 0000.0001_{16}: Timer 1 will initialize again during the next 10 μs. $0000.7FFF_{16}$: Timer 1 needs 327.67 ms until next initialization. $FFFF.FFFF_{16}$: Timer 1 needs 42949.67295 s until next initialization.	0000.0000_{16}	r

Interrupt Registers

The interrupt registers are used to distribute all possible failures or status information to the UPA interrupt concentrator (UIC). The registers are the central areas to enable the interrupts and read back the status of a pending interrupt.

Interrupts are cleared in different ways. The VME ACFAIL and SYSFAIL interrupts, which detect the deassertion of the respective signals, are cleared by writing a 1 to the respective bits in the Interrupt Pending Status Register. All other interrupts are cleared by setting/clearing bits in their respective control registers. In order to clear the timer 1 interrupt, for example, the bit CLR_TIM1 in the Timer Clear Control register must be set to 1.

Interrupt Enable Control Register

This register is used to enable or disable the interrupt sources.

Address: 1FF.F160.0180$_{16}$

Table 40: *Interrupt Enable Control Register*

Bit	Name	Description	Default	Access
0	IE_WDT	Enables the watchdog timer interrupt. 0: Watchdog timer interrupt is disabled. 1: Watchdog timer interrupt is enabled.	0_2	r/w
1	Reserved	This bit is always zero.	0_2	r/w
2	IE_TEMP	Enables the Temperature Interrupt. 0: Temperature interrupt is disabled. 1: Temperature interrupt is enabled.	0_2	r/w
3	Reserved	This bit is always zero.	0_2	r/w
4	IE_TIMER1	Enables the timer 1 interrupt. 0: Timer 1 interrupt is disabled. 1: Timer 1 interrupt is enabled.	0_2	r/w
5	IE_TIMER2	Enables the timer 2 interrupt. 0: Timer 2 interrupt is disabled. 1: Timer 2 interrupt is enabled.	0_2	r/w
6	IE_ACFAIL	Enables the interrupt of the deassertion of the VMEbus ACFAIL signal. 0: ACFAIL interrupt is disabled. 1: ACFAIL interrupt is enabled.	0_2	r/w
7	IE_SYSFAIL	Enables the interrupt of the deassertion of the VMEbus SYSFAIL signal. 0: SYSFAIL interrupt is disabled. 1: SYSFAIL interrupt is enabled.	0_2	r/w

Interrupt Pending Status Register

This register reflects whether a certain interrupt is pending.

Address: 1FF.F160.0184$_{16}$

Table 41: *Interrupt Pending Status Register*

Bit	Name	Description	Default	Access
0	IP_WDT	Reflects if a Watchdog Timer Interrupt is pending 0: No Watchdog timer interrupt is pending. 1: The Watchdog timer interrupt is pending.	0_2	r
1	Reserved	Reserved	0_2	r

Bit	Name	Description	Default	Access
2	IP_TEMP	Reflects if a temperature interrupt is pending 0: No temperature interrupt is pending. The temperature senors did not detect a temperature that exceeds the actual limit. 1: The temperature interrupt is pending. The temperature sensor has detected a temperature above the actual limit.	0_2	r
3	Reserved	Reserved	0_2	r
4	IP_TIMER1	Reflects if a timer 1 interrupt is pending 0: No timer 1 interrupt is pending. 1: The timer 1 interrupt is pending.	0_2	r
5	IP_TIMER2	Reflects if a timer 2 interrupt is pending 0: No timer 2 interrupt is pending. 1: The timer 2 interrupt is pending.	0_2	r
6	IP_ACFAIL	Reflects if a interrupt from the VMEbus ACFAIL signal is pending 0: No ACFAIL interrupt is pending. 1: The ACFAIL interrupt is pending. The interrupt can be cleared by writing a 1 to this bit.	0_2	r/w
7	IP_SYSFAIL	Reflects if a interrupt from the VMEbus SYSFAIL signal is pending 0: No SYSFAIL interrupt is pending. 1: The SYSFAIL interrupt is pending. The interrupt can be cleared by writing a 1 to this bit.	0_2	r/w

Reset Register

The reset register is used to identify the last occurred reset. If all bits are cleared (0), the last reset was a power–on reset. Only one reset status bit can be active at the same time. Every reset clears the previous reset status bit.

Address: 1FF.F160.01D4$_{16}$

Table 42: *Reset Status Register*

Bit	Name	Description	Default	Access
0	RST KEY	Reflects whether the last reset has been generated by the front panel reset key 0: Front panel reset key has not been pressed. 1: Front panel reset key has been pressed.	0_2	r
1	RST SW	Reflects whether the last reset has been generated through software inside the processor 0: No software reset has occurred. 1: Software reset has occurred.	0_2	r
2	RST WD	Reflects whether the last reset has been generated through a watchdog timer time-out condition 0: No watchdog timer reset has been triggered. 1: The watchdog timer reset has been triggered.	0_2	r
3	RST RTB	Reflects whether the last reset has been generated through a push-button reset on the board's IOBP 0: No push-button reset from the CPU board's IOBP has been triggered. 1: Push-button reset from the CPU board's IOBP has been triggered.	0_2	r
4	RST VME	Reflects whether the last reset has been generated through a VMEbus reset 0: No VMEbus reset has been triggered. 1: VMEbus reset has been triggered.	0_2	r
5	RST PMC	Reflects wheather the last reset has been generated through a PMC module 0: No PMC reset has been triggered. 1: PMC reset has been triggered.	0_2	r
7..6	0	Reserved	00_2	r

Board Status Registers

The Board Status registers are used to identify the current configuration of the board. The switch settings can be read from two registers.

Switch 1 and 2 Status Register

This register is used to read the switch settings of switches 1 and 2.

Address: 1FF.F160.01E0$_{16}$

Table 43: *Switch 1 and 2 StatusRegister*

Bit	Name	Switch Setting/Functionality	Default	Access
0	SW1–1	Flash memory write protection 0: ON (Flash memory writing enabled) 1: OFF (Flash memory writing disabled)	1_2	r
1	SW1–2	Boot device selection 0: ON (Boot from Flash memory) 1: OFF (Boot from PLCC PROM)	1_2	r
2	SW1–3	Watchdog enabling 0: ON (Watchdog enabled) 1: OFF (Watchdog disabled)	1_2	r
3	SW1–4	Reset/Abort key enabling 0: ON (Reset/Abort key disabled) 1: OFF (Reset/Abort key enabled)	1_2	r
4	SW2–1	User–defined Switch 0: ON 1: OFF	1_2	r
5	SW2–2	User–defined Switch 0: ON 1: OFF	1_2	r
6	SW2–3	User–defined switch 0: ON 1: OFF	1_2	r
7	SW2–4	User–defined switch 0: ON 1: OFF	1_2	r

Switch 3 and 4 Status Register

This register is used to read the switch settings of switch SW3 and SW4.

Address: 1FF.F160.01E1$_{16}$

Table 44: *Switch 3 and 4 Status Register*

Bit	Name	Switch Setting/Functionality	Default	Access
0	SW3–1	Enable termination for SCSI 1 0: ON (Termination disabled) 1: OFF (Termination enabled)	1_2	r
1	SW3–2	Enable termination for SCSI 2 0: ON (Termination disabled) 1: OFF (Termination enabled)	1_2	r

Bit	Name	Switch Setting/Functionality	Default	Access
2	SW3–3	Enable termination for SCSI 3 (avaliable on I/O board) 0: ON (Termination disabled) 1: OFF (Termination enabled)	1_2	r
3	SW3–4	Reserved 0: ON 1: OFF	1_2	r
5 .. 4	SW4–2 and SW4–1	VME Slot 1 Detection 00_2: SW4–2 ON and SW4–1 ON (VME slot 1 function) 10_2: SW4–2 OFF and SW4–1 ON (VME slot 1 function) 01_2: SW4–1 OFF (Automatic VMEbus slot 1 detection enabled)	11_2	r
6	SW4–3	External VMEbus SYSRESET function 0: ON (VMEbus SYSRESET does not generate board reset) 1: OFF (VMEbus SYSRESET generates board reset)	1_2	r
7	SW4–4	VMEbus SYSRESET generation 0: ON (board reset is not driven to VMEbus SYSRESET) 1: OFF (board reset is driven to VMEbus SYSRESET)	1_2	r

Board Configuration Status Register 1

This register reflects the hardware configuration of the CPU board.

Address: 1FF.F160.01E2$_{16}$

Table 45: *Board Configuration Status Register 1*

Bit	Name	Description	Default	Access
1..0	IO–PRESENT	These bits show whether an I/O board is plugged on the CPU board (if applicable). 0: No I/O board present 1: I/O board present 2: Reserved 3: Reserved	00_2	r
3..2	IOBP–PRESENT	These bits are showing which type of the IOBP–CPU is plugged at the rear side of the CPU board. 0: No IOBP–CPU present 1: IOBP–CPU/3 present 2: IOBP–CPU/5 present 3: Reserved	00_2	r
4	PMC1/2 VIO	This bit is set to 1 if the PMC modules 1 and 2 are configured with a VI/O of 5V (if applicable) 0: PMC1/2 have a VI/O of 3.3V 1: PMC1/2 have a VI/O of 5V	0_2	r
5	PMC3/4 VIO	This bit is set to 1 if the PMC modules 3 and 4 are configured with a VI/O of 5V (if applicable) 0: PMC3/4 have a VI/O of 3.3V 1: PMC3/4 have a VI/O of 5V	0_2	r
6	FKBD/MSE–PRESENT	This bit shows which type of keyboard/mouse is plugged into the front connector. 0: No SUN style keyboard/mouse or a PS/2 style keyboard/mouse is plugged into the front connector. 1: A SUN style keyboard/mouse is plugged into the front connector.	0_2	r
7	RKBD/MSE–PRESENT	This bit shows which type of keyboard/mouse is plugged into the rear connector. 0: No SUN style keyboard/mouse or a PS/2 style keyboard/mouse is plugged into the rear connector. 1: A SUN style keyboard/mouse is plugged into the rear connector.	0_2	r

Board Configuration Status Register 2

This register gives information about additional board conditions.

Address: 1FF.F160.01E3$_{16}$

Table 46: *Board Configuration Status Register 2*

Bit	Name	Description	Default	Access
0	PMC_EREADY	This bit shows the initialization status of a non monarch processor PMC module. PMC_EREADY is a wired OR signal of all PMC modules. 0: At least one of the PMC modules has not completed its initialization cycle. 1: All PMC modules have completed their initialization and are able to respond to configuration cycles from the host processor.	1_2	r
7..1	–	Reserved	0000000_2	r

Hardware Revision Register

The Hardware Revision register is used to identify current PCB and FPGA revision.

Address: 1FF.F160.01EF$_{16}$

Table 47: *Hardware Revision Register*

Bit	Name	Description	Access
7..0	HW REVISION	Status of the Board 00_{16}: PCB revision: 1.0 and FPGA revision: 0_{16} 01_{16}: PCB revision: 1.0 and FPGA revision: 1_{16} 02_{16}: PCB revision: 1.0 and FPGA revision: 2_{16} 10_{16}: PCB revision: 1.1 and FPGA revision: 10_{16} 11_{16}: PCB revision: 1.1 and FPGA revision: 11_{16} 12_{16}: PCB revision 1.2 and FPGA revision 12_{16} 13_{16} – FE_{16}: Reserved FF_{16}: No valid hardware revision	r

I2C Registers

The I²C registers implemented in the FPGA are used to access the local I²C bus for the SPD, BIBs and temperature sensors.

Address: 1FF.F160.01FE$_{16}$

Table 48: *I2C 1 Register*

Bit	Name	Description	Default	Access
0	I2C–DATAIN 1	This register bit reflects the current status of the I^{2}C–1 data line. 0: I^{2}C–1 dataline is 0. 1: I^{2}C–1 dataline is 1.	–	r
1	I2C–CLK1	This bit corresponds to the I^{2}C clock line and must be set by software to toggle the I2C clock. 0: I^{2}C–1 clock is 0. 1: I^{2}C–1 clock is 1.	–	w
2	I2C–DATAO UT1	This bit is used by software to write to the I^{2}C dataline. 0: The I^{2}C–1 dataline is driven low. 1: The I^{2}C–1 dataline is driven high by an external pull–up.	1_2	r/w
7..3	–	Reserved	00000_2	r/w

Address: 1FF.F160.01FF$_{16}$

Table 49: *I2C 2 Register*

Bit	Name	Description	Default	Access
0	I^{2}C–DATAIN2	This register bit reflects the current status of the I^{2}C–2 data line. 0: I^{2}C–2 dataline is 0. 1: I^{2}C–2 dataline is 1.	–	r
1	I^{2}C–CLK2	This bit corresponds to the I^{2}C clock line and must be set by software to toggle the I^{2}C clock. 0: I^{2}C–2 clock is 0. 1: I^{2}C–2 clock is 1.	–	w
2	I^{2}C–DATAOU T2	This bit is used by software to write to the I^{2}C dataline. 0: The I^{2}C–2 dataline is driven low. 1: The I^{2}C–2 dataline is driven high by an external pull–up.	1	r/w
7..3	–	Reserved	00000_2	r/w

A

Troubleshooting

Error List

A typical VMEbus system is highly sophisticated. This chapter can be taken as an error list for detecting erroneous system configurations and strange behaviors. It cannot replace a serious and sophisticated presales and postsales support during application development.

If it is not possible to fix a problem with the help of this chapter, contact your local sales representative or Field Application Engineer (FAE) for further support.

Problem	Possible Reason	Solution
Board does not work	The 5V backplane voltage is too low.	Check that all backplane voltages are within their specific ranges. Check that power supply is capable to drive the respective loads.
Board does not work (LED1 is OFF and LED3 shines weak red)	The 12V backplane voltage is missing or too low.	Check that all backplane voltages are within their specific ranges. Check that the power supply is capable to drive the respective loads.
Board does not start (LED1 blinks green and LED3 is OFF)	No OpenBoot code was found.	Insert a valid PLCC OpenBoot PROM and set switch 1–2 to OFF. If you are sure to have a valid OpenBoot code in the flash memory, set the switch 1–2 to ON.
VME transfers have failures	There are no or more than one board in the VME system configured as slot 1.	Check all boards for their slot 1 configuration. Only one board must be configured as slot 1. Set switch SW4–1 of the board to OFF for an automatic slot 1 detection.
	VME connectors defect	Check VME P1 and P2 connectors for bent or broken pins. Adjust bend pins, if possible, or replace board.

Problem	Possible Reason	Solution
	VMEbus timeout too short	Increase the timeout of the Bus Timer. The VMEbus handles abnormal bus cycles by asserting the BERR signal. The timeout should be longer than the longest expected bus cycle.
Board does not boot	Wrong boot device	Check the OpenBoot property boot-device. This property must be set to the device (disk, net, cdrom) from which you want to boot. Use the commands probe-scsi and probe-ide to examine the system for boot devices
	SCSI bus not terminated	Check the SCSI cable for proper termination. Check also switch SW-3 of the board for correct SCSI bus termination.

B

Battery Exchange

Battery Exchange

The battery provides data retention of seven years summing up all periods of actual data use. Force Computers therefore assumes that there usually is no need to exchange the battery except, for example, in case of long–term spare part handling.

Caution

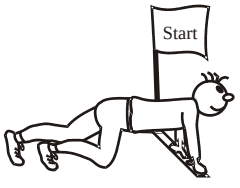
- **Board/System damage**
  Incorrect exchange of lithium batteries can result in a hazardous explosion. Therefore, exchange the battery as described in this chapter.

- **Data loss**
  If the battery does not provide enough power anymore, the RTC is initialized and the data in the NVRAM is lost. Therefore, exchange the battery before seven years of actual battery use have elapsed.

- **Data loss**
  Exchanging the battery always results in data loss of the devices which use the battery as power backup. Therefore, back up affected data before exchanging the battery.

- **Data loss**
  If installing another battery type than is mounted at board delivery may cause data loss since other battery types may be specified for other environments or may have a shorter lifetime. Therefore, only use the same type of lithium battery as is already installed.

Exchange Procedure



1. If battery is covered by I/O board, remove I/O board first

Caution

PCB and battery holder damage
Removing the battery with a screw driver may damage the PCB or the battery holder. To prevent this damage, do not use a screw driver to remove the battery from its holder.

2. Exchange battery
3. When installing new battery, ensure that battery connectors fit sockets on CPU board
4. Install battery in such a way that the dot marked on top of battery covers dot marked on chip.
5. If necessary, reinstall I/O board

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Product Error Report

Product:	Serial No.:
Date Of Purchase:	Originator:
Company:	Point Of Contact:
Tel.:	Ext.:
Address: _____ _____ _____	
Present Date:	
Affected Product: O Hardware O Software O Systems	Affected Documentation: O Hardware O Software O Systems
Error Description: _____ _____ _____ _____ _____ _____ _____ _____ _____	
This Area to Be Completed by Force Computers: Date: PR#: Responsible Dept.: O Marketing O Production O Eng. (Board) O Eng. (Systems)	

Send this report to the nearest Force Computers headquarter listed on the address page.