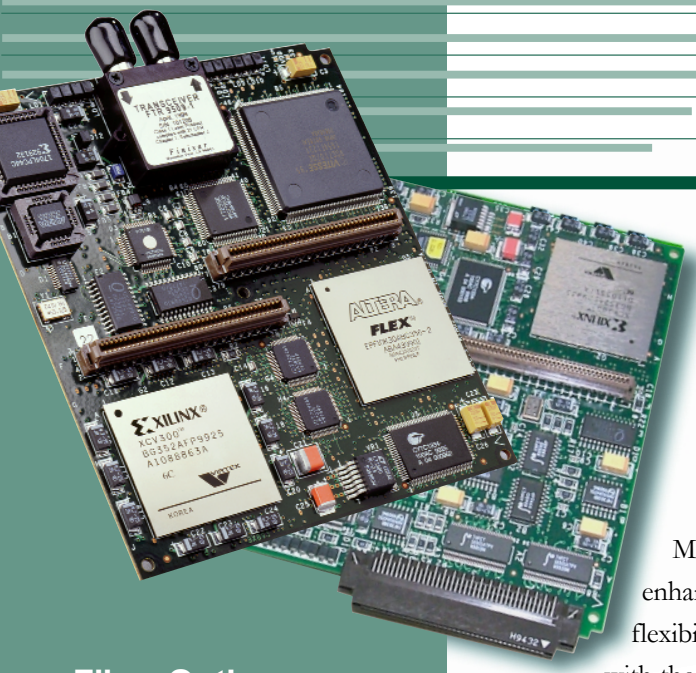


Computer Systems, Inc.
MERCURY

RACE++ Series

RINOJ I/O Daughtercards

Fiber-Optic or Copper TTL FPDP

160 MB/s Sustained Input or Output Over Copper

Up to 100 m Connections over Optical Fiber

Real-Time Latency as Low as 4 µs

Support for All Four FPDP Data Modes

Linked-List DMA Distributes Data with No Processor Intervention

Data-Directed DMA Supports Sensor Mode Changes

Mercury brings enhanced performance and flexibility to external I/O with the RINOJ I/O daughtercards. Available for versatile fiber-optic or maximum-speed TTL copper-based cabling, these products are ideally suited as the real-time digital interface for sensor input or data output in a RACE™ or RACE++™ system.

RINOJ I/O daughtercards implement the Front Panel Data Port (FPDP) protocol for high-performance data I/O devices. The 32-bit TTL version implements all four FPDP modes and operates at 160 MB/s, the highest speed possible under FPDP. The fiber-optic version implements the serial version of FPDP currently in the VITA standardization process. This provides up to 105 MB/s of I/O over cables up to 100 meters.

Full Compatibility

The RINOJ daughtercards are the high-performance RACE++ successors to the RIN-T™ and ROUT-T™ product line. Both versions of the RINOJ daughtercards are compatible with the RACE and RACE++ architectures. This eases migration from the older I/O daughtercards while offering significant improvements in performance, functionality, and flexibility.

The parallel TTL version is also compatible with more than a hundred existing FPDP products. All four FPDP framing modes are supported for ultimate compatibility.

I/O Intelligence

The RINOJ is more than an ordinary digital interface – it has the smarts to distribute the data where you want it without processor intervention. The RINOJ can sense signals in the input data stream that indicate sensor mode changes, and route data appropriately for each different mode.

Sensors indicate their mode through an optional word in the data header. Each mode can be made to correspond with an application-defined DMA command packet (CP) chain on the RINOJ. These command packets cause the RINOJ's DMA controller to route the data to a predefined destination anywhere on the RACEway fabric.

DMA command packets can be chained together to automatically distribute subsequent data packets to different processors or endpoints on the RACEway fabric. This feature can be combined with RACEway broadcast and multicast features that can send the same data packet to multiple processors, providing complete flexibility in intelligent data distribution.

RACE++ SERIES

Fiber or Copper: Your Choice

Mercury's RINOJ product family adds fiber-optic capabilities to Mercury's earlier copper-based products. This lets you select between the intrinsic advantages of copper wire or fiber-optic communications paths.

- Copper cables support data streams of parallel communications, allowing them to operate at 160 MB/s. This makes copper the ideal medium in applications calling for a small number of input streams running a short distance that demand the highest data rate.
- Optical cables and their connectors take up less space than their copper-based counterparts, making it easier to get a large number of them into a chassis. Optical fiber also resists electromagnetic interference (EMI) and is not susceptible to ground loops. Most importantly, optical fiber allows connections that span up to 100 meters. This makes fiber-optic cabling the preferred solution for a large number of data streams, sensors separated from processing chassis by long distances, or environments in which EMI is an issue.

RACE++ Interface

The RINOJ daughtercards include a RACE++ interface for high-performance data transfer to and from the processing system over the RACEway interconnect fabric. This interface can provide data transfer in bursts up to 267 MB/s to the RACE++ motherboard, a speed far greater than the maximum FPDP data rate. When connected to a RACE motherboard, data transfers in bursts up to 160 MB/s.

Continuous transfer rates are currently limited by the media used to transfer data to or from the board. In the case of the fiber-optic version, the excess capacity through the RACEway interface can be used to facilitate a bi-directional interface.

RINOJ-T: Parallel TTL Interface (FPDP)

The RINOJ-T (see Figure 1) brings an FPDP data stream into a RACEway system via copper ribbon cable. In a RACE++ system with a RACEway clock of 66.66 MHz, the RINOJ-T can operate at a sustained input or output rate of 160 MB/s (the maximum for FPDP). When used in either a RACE or RACE++ system operating with a RACEway clock of 40 MHz, the maximum data rate is 120 MB/s.

The RINOJ-T supports all four framing options specified by the FPDP specification (ANSI/VITA 17-1998) as follows:

- **Unframed** - The data is not framed. The design of the application includes using predetermined data transfer sizes and coordination of the start of the data stream.
- **Single-Frame Data** - Data is framed through the use of the FPDP signal SYNC* at the start of each transmission (DVALID* is not asserted at the same time). Here the RINOJ can be configured to start taking data when a SYNC* arrives, intended to occur once per transmission.
- **Dynamic-Size Repeating Frame Data** - Data is framed through the assertion of SYNC* and DVALID* together at the end of an FPDP frame of data. The FPDP frame size can vary from one frame to the next. The RINOJ can be configured to end the DMA transfer with the cur-

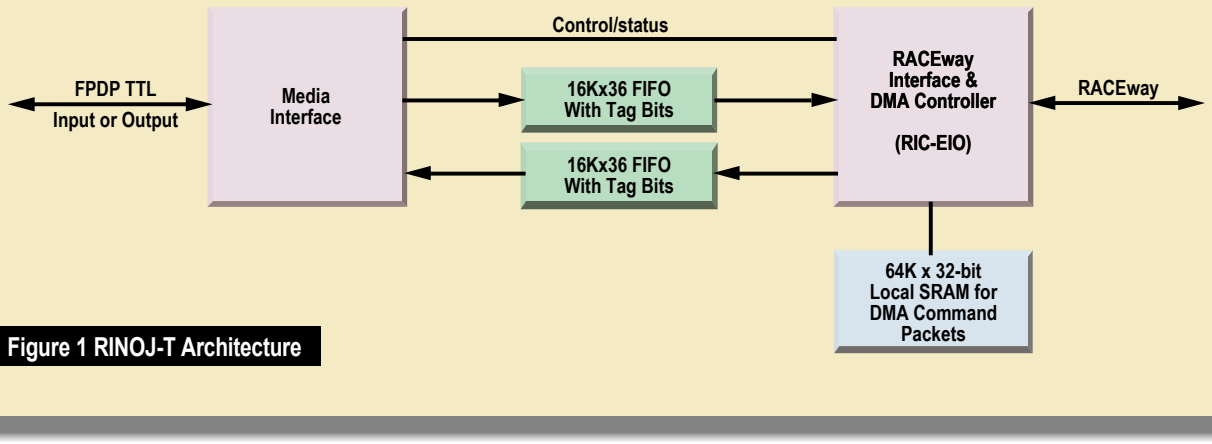


Figure 1 RINOJ-T Architecture

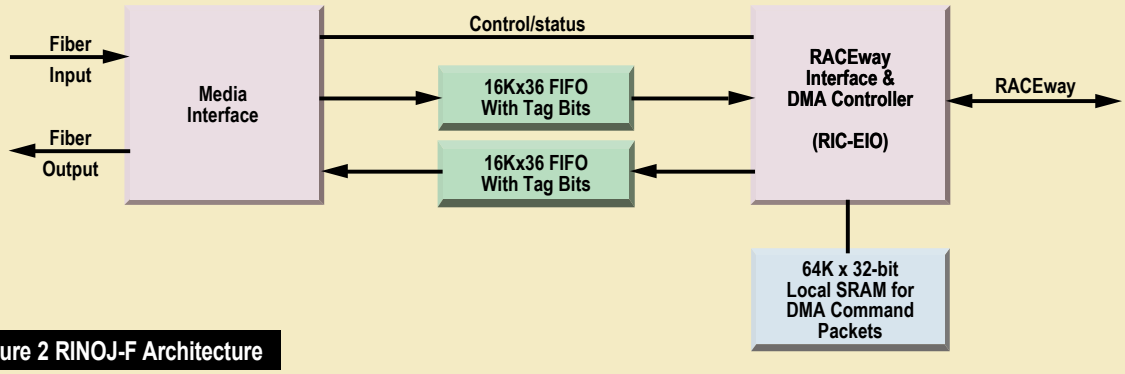


Figure 2 RINOJ-F Architecture

rent command packet upon receipt of these end-of-frame signals and be notified of the amount of data actually received. The RINOJ can also branch to another command packet upon the end of an FPDP packet.

- **Fixed-Size Repeating Frame Data** - Data is framed through the assertion of SYNC* and DVALID* together at the end of an FPDP frame of data. This is the same as Dynamic-Size Repeating Frame Data, except that the frame size is not permitted to vary. The RINOJ-T treats this in the same manner as Dynamic-Size Repeating Frame Data.

RINOJ-F: Fiber-Optic Interface

The RINOJ-F supports a mapping of the FPDP protocol onto the Fibre Channel physical layers (FC-0 and FC-1). Using this serial FPDP protocol, the RINOJ-F supports the same framing options as the RINOJ-T.

Serial data is transmitted at 1.0625 Gbaud over the fiber. This enables a sustained data rate of 105 MB/s when the data packets are kept large on both the fiber side and the RACEway side of the interface.

The serial protocol provides error checking and optional flow control. Error checking is accomplished with a CRC (cyclic redundancy check) included with each packet sent over the serial line. The optional flow control feature enables the receiving end of the fiber interface to send flow control command through its output port back to the data transmitter. If flow control is not used, only a single fiber per data channel is required.

Compatible with FibreXtreme

The serial protocol used by the RINOJ-F is directly compatible with Systran's line of FibreXtreme™ products. These products will include a variety of 6U VME, CMC (common mezzanine card), PMC, and PCI interfaces.

In addition to providing a method to move streams of data, with high throughput between systems from Mercury and those from other vendors, compatibility with FibreXtreme can shorten design, implementation, and debugging time. For example, a FibreXtreme CMC provides an off-the-shelf module that can be integrated into a sensor as a digital interface at the data source. During system debugging, a PC with a FibreXtreme PCI interface can act as a data source or sink to emulate the interface between the RINOJ-F and sensors.

RINOJ-F Bi-directional Operation

Although generally operated as either an input device or an output device, the RINOJ-F is capable of bi-directional data transfers. On the fiber side of the FIFOs, the RINOJ-F is full duplex. The FIFOs are capable of simultaneous input and output (see Figure 2). On the RACEway side of the FIFOs, the RINOJ-F has a single DMA controller that is shared for both input and output.

DMA chains that move data in both directions can be created with some CPs moving data in and some moving data out. The direction of data movement is controlled by a bit in the DMA CP. Contact Mercury for more information on the transfer control required to keep that data flowing.

RINOJ-F Copy Mode

The RINOJ can also loop any data arriving through its receive fiber directly onto its transmit fiber. Copy mode is useful for systems in which it is desirable to record the incoming data. When copy mode is enabled, the data can be both stored to nodes on the processor containing the RINOJ-F as well as passed on to a test chassis for recording. Because copy mode uses the RINOJ-F transmit fiber to send a copy of the input stream, both flow control and data output by the RINOJ-F are disabled when copy mode is enabled. Copy mode is enabled via a bit in a RINOJ-F control register that is accessed by the I/O management software.

I/O Management Software

Mercury provides a data transfer facility layered on top of the standard Mercury MC/OS™ runtime environment. This facility consists of a set of user-callable I/O control functions. These functions are used to define I/O transfer requests (DMA command packets) and to link such requests into a chain that is then automatically executed by the designated I/O device.

Each CP specifies the RACEway route, address, and maximum word count for the transfer as well as some control information. The route in each CP can specify either a single RACEway endpoint or, in the case of an input stream, a multicast to multiple RACEway endpoints. By chaining CPs together into a linked list, an incoming stream can be parceled out among a large number of endpoints. Transfers of up to 8 MB in length may be implemented.

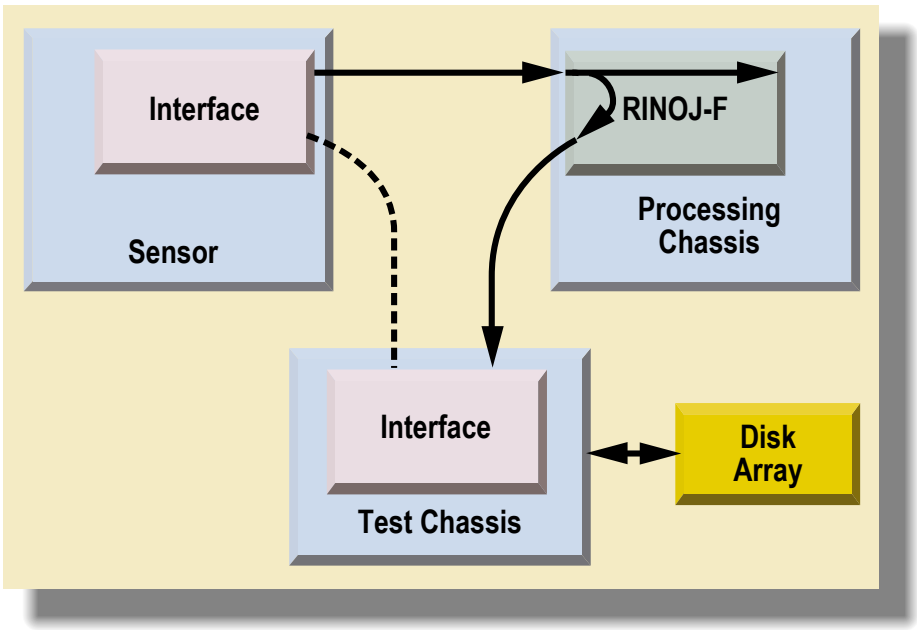
The requests can be chained, with the option of synchronization at the end of each chain. Synchronization between the RINOJ and the application program can be accomplished by queuing a transfer request that transfers status information at the desired synchronization point in the DMA chain. This block of status information is written to the local memory of the processor with which it is being synchronized. The processor can then poll on a location in the block of status information. The RINOJ also can be synchronized with a processor when set up to send a mailbox interrupt to the desired processor.

Linked-List DMA Controller

The RINOJ daughtercards include a linked-list DMA controller for intelligent control of data distribution. The linked-list DMA controller is controlled by lists of DMA CPs. Since they are constructed once at setup time and can be initiated multiple times within the time-critical portion of the application, such chains of transfer requests are very valuable for repetitive, high-speed transfers. In many applications, once the DMA controller is set up it can run autonomously, scattering or gathering data among a large number of processing nodes with no processor intervention.

The DMA CPs are stored in an SRAM local to the RINOJ to reduce latency. This local SRAM is 64K x 32 bits, allowing more than 8,000 CPs to be stored.

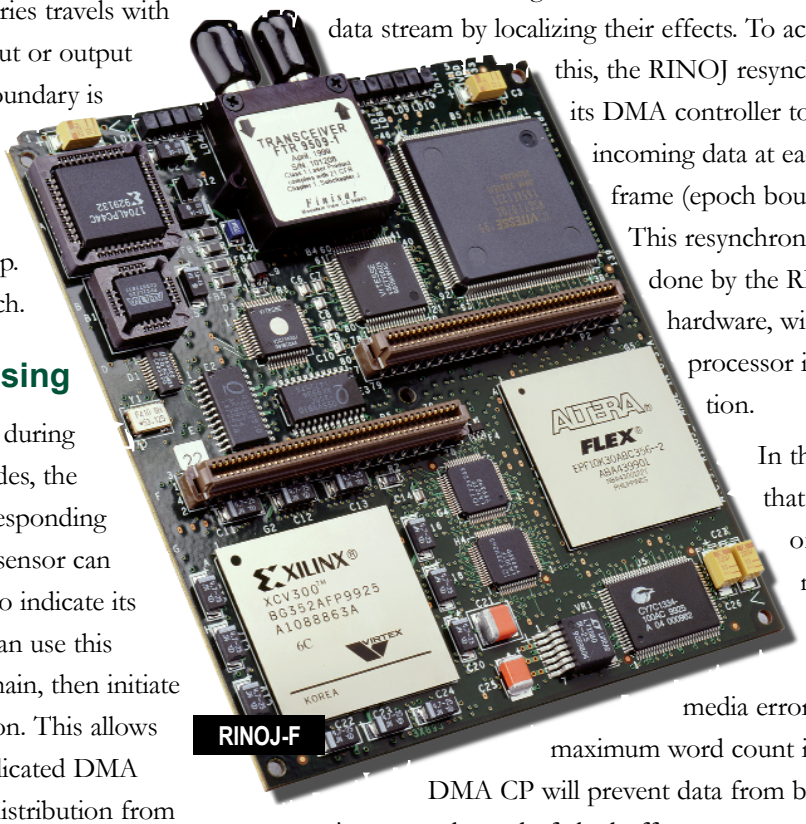
Figure 3 Example RINOJ-F Copy Mode Configuration



Data Frame Management

The RINOJ allows the sensor to frame the data into "epochs." Any sensor can define its own epoch boundary based on what makes sense for that type of sensor and on how the data will be used by the processing system. In the case of radar data, these epochs are likely to be coherent processing intervals. In the case of images, an epoch is likely to be the frame of an image.

Information about the epoch boundaries travels with the data. When data is stored in an input or output FIFO, a tag bit indicating the epoch boundary is stored with the data. A typical use of this feature is storing images. A line of an image is stored to multiple endpoints at each pass through the loop. In this case, the entire image is an epoch.



RINOJ-F

Data-Driven Frame Processing

Many modern sensors change modes during operation. When a sensor changes modes, the processing system must make the corresponding mode change at the correct time. The sensor can also use the first word of each epoch to indicate its current mode. The RINOJ hardware can use this word to select a particular DMA CP chain, then initiate the chain without processor intervention. This allows each mode of the sensor to have a dedicated DMA chain and a completely different data distribution from other modes.

The DMA controller also contains a next-chain register, which can be used by a processor to select the chain to use for the next epoch. This allows the handling of multiple modes in cases where it is not practical to include a header in the input data stream.

DMA Controller Offset Register and Looping

The RINOJ DMA controller contains offset registers that can be used for incrementing through a set of buffers on the destination or source nodes. A chain of CPs can be created that loops on itself. The last CP in the loop can be set up to add a delta to the offset register each time through the loop. This offset register can be added to the address specified by the CPs. In many cases this allows the required number of CPs to be reduced significantly.

Recovering from Input Stream Faults

With some input interfaces, missing or extra data can cause the interface to become out of sync with an input data stream until a processor intervenes. The RINOJ minimizes the damage due to anomalies in the input data stream by localizing their effects. To accomplish this, the RINOJ resynchronizes its DMA controller to the incoming data at each data frame (epoch boundary). This resynchronization is done by the RINOJ hardware, with no processor intervention.

In the event that an end-of-epoch marker is lost due to a media error, the maximum word count in the DMA CP will prevent data from being written past the end of the buffer.

Extremely Low Latency for Input Data

The RINOJ can be configured to give a latency of less than 4 □s from when data arrives at the interface to when it is on a processing node ready to be processed. The main feature that enables this low latency is the linked-list DMA CP processing of the RINOJ's DMA controller. By cycling through lists of DMA commands set up during initialization, the RINOJ can autonomously distribute the data without any processor intervention.

Two additional features ensure that low-latency operation is maintained. First, a programmable threshold is used to tell the DMA controller when it should start

emptying its input FIFO. If the FIFO has more than the specified amount of data, the DMA controller will start emptying the FIFO. Second, the RINOJ includes a programmable timer that will cause any remaining data to be emptied from the input FIFO if no input data arrives for the specified length of time.

Connecting Loosely Coupled Systems

In some cases, applications can benefit from having the system split into multiple, loosely coupled chassis to provide isolation among subsystems. RINOJ interfaces can be used to facilitate the point-to-point connections for such a system.

Generally it is desirable to have a DMA controller at both ends of the connection. One chassis cannot communicate with a remote chassis unless the DMA controller of the remote chassis is set up to take in the data, thereby achieving the desired isolation.

Configuration Options

Media

RINOJ-F:	**Optical Fiber**
RINOJ-T:	**Parallel TTL**

Front Panels

Each RINOJ-F and RINOJ-T come with a front panel to adapt to the motherboard: Please specify board model (e.g., MCJ6)

Cables

RINOJ-F:	**Each I/O board includes a "test" cable**
RINOJ-T:	**Each I/O board includes a cable**
	Please specify desired length: 10 inches or 2 meters

Mercury also offers connector plugs and receptacles for mounting on your custom acquisition device and cable, respectively.

910-04005:	**IOT-P, connector plug for mounting on the board, compatible with RINOJ-T cables. This plug is used for mounting on customer-designed boards.**
910-04006:	**IOT-R, connector receptacle for RINOJ-T cable, compatible with RINOJ-T board connections. This plug can be used to make custom cables.**

Configuration Requirements

RACE and RACE++ Series Motherboards

RINOJ-F:*	**MCH9™, MCJ6, MCJ9, MultiPort™ and its successor**
RINOJ-T:	**MCH6™, MCH9, MCJ6, MCJ9, MultiPort and its successor**

* RINOJ-F is not compatible with MCH6 due to mechanical interference with the fiber-optic transceiver.

MC/OS Runtime Environment

RINOJ-F:	**MC/OS 5.3 or later***
RINOJ-T:	**MC/OS 5.3 or later***

* RINOJ daughtercards include a driver software package for MC/OS.

Electrical/Mechanical Specifications

Memory Sizes

Input FIFO size:	**16K x 36 bits***
Output FIFO size:	**16K x 36 bits***
SRAM for DMA command packets:	**64K x 32 bits**

* 32 bits of the width is for data and 4 bits is used to tag the data with labels such as "end-of-epoch."

RINOJ-F Media

Wavelength:	**850 nm (shortwave)**
Data rate:	**1.0625 Gbaud**
Multi-mode fiber:	**62.5/125 um or 50.0/125 um**
Connector type:	**ST**
Distance*:	**100 m**

* For distances over 100 m, consult Mercury.

RINOJ-T Media (FPDP)

Specification:	**ANSI/VITA 17-1997**
Mating Connector:	**KEL 8825E-080-175**

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