EPC®-6315 Hardware Reference

www.radisys.com

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Before you begin

This guide describes EPC-6315, a PrPMC (Processor PCI Mezzanine Card) that uses the RadiSys 82600 integrated chipset to bring an Intel† Architecture processor into ultra-dense form factors. This guide is for hardware and software designers, engineers, and those with a electronics and/or programming knowledge who need to understand the EPC-6315 operation.

About this guide

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Chapter/appendix	Description
G Carrier card design	Provides guidelines for designing a carrier card that supports Monarch mode.
H EPC-6315 test board	Provides guidelines for designing a a full ATX sized, four PMC site circuit board to begin production, test, and early development using the EPC-6315.

Notational conventions

This manual uses the following conventions:

- `Screen text and syntax strings appear in this font.`
- All numbers are decimal unless otherwise stated.
- Bit 0 is the low-order bit. If a bit is set to 1, the associated description is true unless otherwise stated.


Notes indicate important information about the product.


Tips indicate alternate techniques or procedures that you can use to save time or better understand the product.


The globe indicates a World Wide Web address.


The book indicates a book or file.


ESD cautions indicate situations that *may* cause damage to hardware via electro-static discharge (ESD).


Cautions indicate potentially hazardous situations which, if not avoided, *may* result in minor or moderate injury, or damage to data or hardware. It may also alert you about unsafe practices.


Warnings indicate potentially hazardous situations which, if not avoided, *can* result in death or serious injury.


Danger indicates imminently hazardous situations which, if not avoided, *will* result in death or serious injury.

Where to get more information

About EPC-6315

You can find out more about EPC-6315 from these sources:

- **Readme file:** Lists features and issues that arose too late to include in other documentation.
- **World Wide Web:** RadiSys maintains an active site on the World Wide Web. The site contains current information about the company and locations of sales offices, new and existing products, contacts for sales, service, and technical support information. You can also send e-mail to RadiSys using the web site.


When sending e-mail for technical support, please include information about both the hardware and software, plus a detailed description of the problem, including how to reproduce it.

To access the RadiSys web site, enter this URL in your web browser:
http://www.radisys.com

Requests for sales, service, and technical support information receive prompt response.

- **Other**: If you purchased your RadiSys product from a third-party vendor, you can contact that vendor for service and support.

About related RadiSys products

82600 High Integration Dual PCI System Controller Data Book: This book details the RadiSys 82600 High Performance System Controller, a member of the RadiSys family of long-life embedded PC compatible core logic. The 82600 is a highly integrated single chip implementation of all requirements of a high performance Compact PCI Central Resource and Peripheral Bridge including the North Bridge, South Bridge, PCI to PCI Bridge, and a selected set of Super I/O functions targeted at embedded, PC-compatible systems. It supports Intel Celeron†, Pentium II, and Pentium III processors with 66MHz, 100MHz and 133MHz system bus frequencies.

About related EPC-6315 components

Processor PMC standard, VITA 32-199X, Draft 0.41

PCI Specification, Revision 2.2

Other

- For MV Linux† LSPs, contact MontaVista at this URL:

  http://www.mvista.com

- For VxWorks† BSPs, contact RadiSys or WindRiver

  http://www.windriver.com
  http://www.radisys.com

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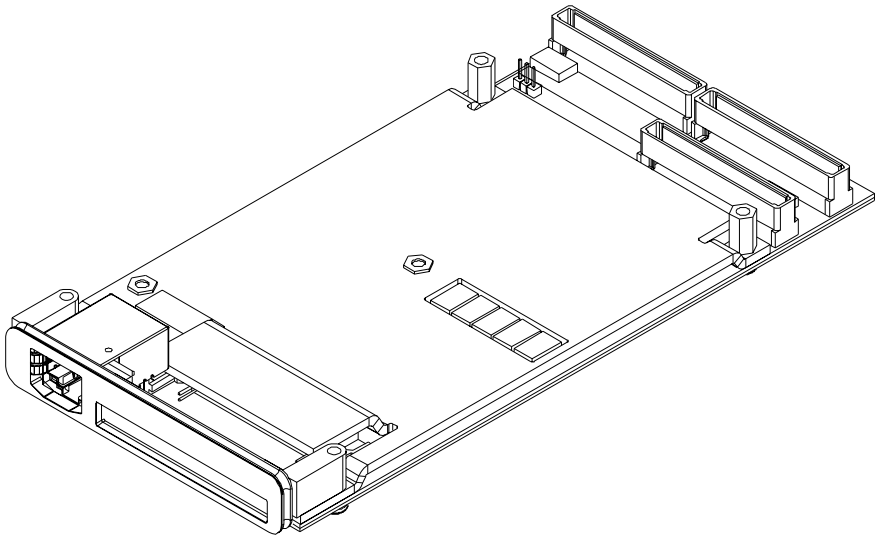
1 Introduction

The EPC®-6315 PrPMC (Processor PCI Mezzanine Card) uses the RadiSys 82600 integrated chipset to bring an Intel Architecture processor into ultra-dense form factors. With the ability to accept a type I Compact Flash device, the EPC-6315 can be a completely self-standing processor in any application.

The EPC-6315 includes an 800MHz Pentium III processor with up to 512MB of on-board SDRAM. The EPC-6315 also features ECC protection of memory with single-error correction and double-error detection capability. Performance is maximized with the standard 133MHz PSB and 133MHz memory bus. For maximum flexibility, the EPC-6315 leverages the dual mode PCI-to-PCI bridge capability of the RadiSys 82600 to automatically configure the bridge based on the strapping of the slot on the baseboard. This capability allows the EPC-6315 to become a Monarch PrPMC, and provide PCI bus enumeration and service interrupts on the PCI bus or a non-Monarch PrPMC and function as a PCI-based auxiliary processor.

The Jn1 and Jn2 connectors provide a 32-bit 33/66MHz interface to the PCI bus on the baseboard as well as providing power and ground. The optional Jn4 connector provides a full set of I/O, which includes EIDE, COM, and keyboard/mouse interfaces. The front panel provides 10/100BASE-T Ethernet connector and Compact Flash socket.

Figure 1-1. The EPC-6315



You can order the EPC-6315 in these configurations:

Configuration	Description	Memory IC capacity	No. IC chips
EPC6315-800-256	256 MB SDRAM	32 Mb x 8	9
EPC6315-800-512	512 MB SDRAM	64 Mb x 8	9

Features

The EPC-6315 includes:

Compatibility

- Compatible with *Processor PMC standard, VITA 32-199X, Draft 0.41*

Intel Tualatin LP processors in micro-FCBGA package

- 800 MHz core frequency.
- 133 MHz PSB (Processor Side Bus) frequency.
- 512 KB secondary (L2) cache.
- Switching power supply for CPU core voltage; linear supplies for interface voltages.

CPU subsystem

- RadiSys 82600 dual PCI embedded system controller:

  For detailed information about the 82600 chip, see the *82600 High Integration Dual PCI System Controller Data Book.*

  - Dual independent PCI bus architecture.
  - Monarch and non-Monarch capability on external PCI bus.
  - Memory controller with direct BIOS flash support.
  - Two 82C59 interrupt controllers.
  - 82C54 timer/counter.
  - 74LS612 address mapper.
  - PS/2 compatible keyboard/mouse port.
  - SMBus host interface.
  - Two 82C37 DMA controllers.
  - Real-time clock.
  - COM port support with 16550 compatible UART.
  - Integrated watchdog timer.
- Clock generator and SDRAM clock buffer supporting 133 MHz host clocks and PCI clocks.

- On-board memory capacity: up to 512 Mbytes of PC-133 compliant SDRAM.
- 32 Mb (4 MB) 3V Intel Strata Flash memory.

I/O

- Intel PCI Ethernet controller independently supporting 10BASE-T or 100BASE-TX.
- Compact Flash.

Connectors

- **Carrier card**
  - Jn1 and Jn2 connectors
    Provide a 32-bit 33/66 MHz interface to the PCI bus on the baseboard, plus provides a power and ground state compatible with the Processor PMC draft standard.
  - Jn4 connector (optional)
    Provides a full set of I/O, including EIDE, COM, and keyboard/mouse interfaces.
  - 3-pin header
    Provides access to the system BIOS.
- **Front panel**
  - RJ-45 connector.
  - 10/100BASE-T Ethernet connector
    To simplify network connections, this connector is available on the front panel.
  - Compact flash socket
    Accommodates a Type I compact flash card. With the ability to accept a Type I Compact Flash device, the EPC-6315 can be a completely self-standing processor in any application.

Specifications

Environmental

The EPC-6315 meets the following environmental specifications.

- The EPC-6315 is for use only with compatible UL listed computers that have installation instructions detailing user installation of card cage accessories.
- The operating environment must provide sufficient airflow (200 LFM) across the CPU board to keep it within its temperature specification. Failure to provide sufficient airflow may result in CPU failure.

The maximum temperature decreases when the relative humidity exceeds 30%.

Table 1-1. Environmental specifications

Parameter	Conditions	Detailed specification
Temperature (ambient)	Operating	+5°C to 50°C derated 2°C per 1000 ft (300 m) over 6600ft (2000m) with 200 LFM airflow.
	Storage	–20°C to +60°C.
Relative humidity	Operating	20% to 90% non-condensing 20% per hour maximum excursion gradient..
	Storage	5% - 95% non-condensing 20% per hour maximum excursion gradient.
EMC[1] radiated emission	Operating	EN 55022:1998, Class B.
Conducted emissions	Operating	EN 55022:1998, Class B.
Vibration	Operating	0.04g^2/Hz from 5 to1000 Hz random, 10 min per sweep cycle.
	Storage	0.04g^2/Hz from 5 to1000 Hz random, 10 min per sweep cycle.
Shock, (un-packaged)	Operating	5g, 11ms, half-sine.
	Storage	15g, 11ms, half-sine.
MTBF		309,298 hours at 50°C using Bellcor Issue 6.
Immunity		
ESD[1]	Operating	(All performance criteria from IEC 1000-4-2/EN61000-4-2:1995): 8KV direct contact, performance criteria B. 15 KV air discharge, performance criteria B.
Radiated[1]	Operating	(Performance criteria A from IEC 1000-4-3/EN61000-4-3:1995). Test Level 3V/m and 10V/m.
Surge	Operating	(Performance criteria B from IEC 1000-4-4/EN61000-4-4:1995). Test Level 0.5kV.
Voltage dips and interruptions	Operating	(From IEC 1000-4-11/EN61000-4-11:1995): >95% dip, 10ms—Performance criteria B. 30% dip, 500ms—Performance criteria C. >95% dip, 5000ms—Performance criteria C.
Conducted	Operating	(Performance criteria A from IEC 1000-4-6/EN61000-4-6:1995).
Fast transient/burst	Operating	(Performance criteria B from IEC 1000-4-4/EN61000-4-4:1995): Test Level 0.5kV.

[1] These are system level tests. Conformance of the product to these specifications may be affected by the complete system's ability to conform.

Additional specifications

Table 1-2. Additional EPC-6315 specifications

Characteristic	Value	
Mechanical	Dimensions[1]	74.0 mm x 149.00 mm
	Height, component side First 31mm Remainder	 9.5mm 4.7mm, maximum
	Height, solder side[2]	3.5mm (this includes the 1.6mm board thickness)
	Thickness	1.6 mm
	Component surface to host component surface	10 mm
Heat sink	Provides sufficient cooling for the CPU when used in an environment providing 200 LFM airflow at a maximum temperature of 50° C (air coming into the chassis).[3]	

1 The mechanical outline of the PrPMC module conforms to the dimensions defined by a single wide, standard length PMC module.

2 Measured from the component side for single slot CompactPCI use.

3 The customer assumes the responsibility for doing a detailed thermal analysis for the CPU board on this carrier.

2 Configuration and installation

This chapter describes how to install an EPC-6315 PMC on a RadiSys EPC board.

Avoid causing ESD (electrostatic discharge) damage by following these conventions:

- Keep the blade in its anti-static bag until you are ready to install it.
- Install the blade (as described later in this chapter) only in a static-free environment:
  - Before touching the blade, attach an ESD wrist strap to your wrist and connect its other end to the ESD friction-lock connector at the shelf's lower left.
  - Remove the blade from its antistatic bag only in a static-free environment.
  - Avoid touching printed circuits, connector pins, and components. Where possible, hold the blade only by its edges or mounting hardware.
  - Make the least possible movement with your body to minimize electrostatic charges created by contact with clothing fibers, carpet, and furniture.
  - Keep one hand on the shelf, if possible, as you insert or remove a blade.
  - Avoid placing the blade on the shelf cover or on a metal table. The cover and metal table increase the risk of damage because they provide an electrical path from your body through the blade.

The EPC-6315, like most other electronic devices, is susceptible to ESD damage. ESD damage is not always immediately obvious. It can cause a partial breakdown in semiconductor devices that might not result in immediate failure.

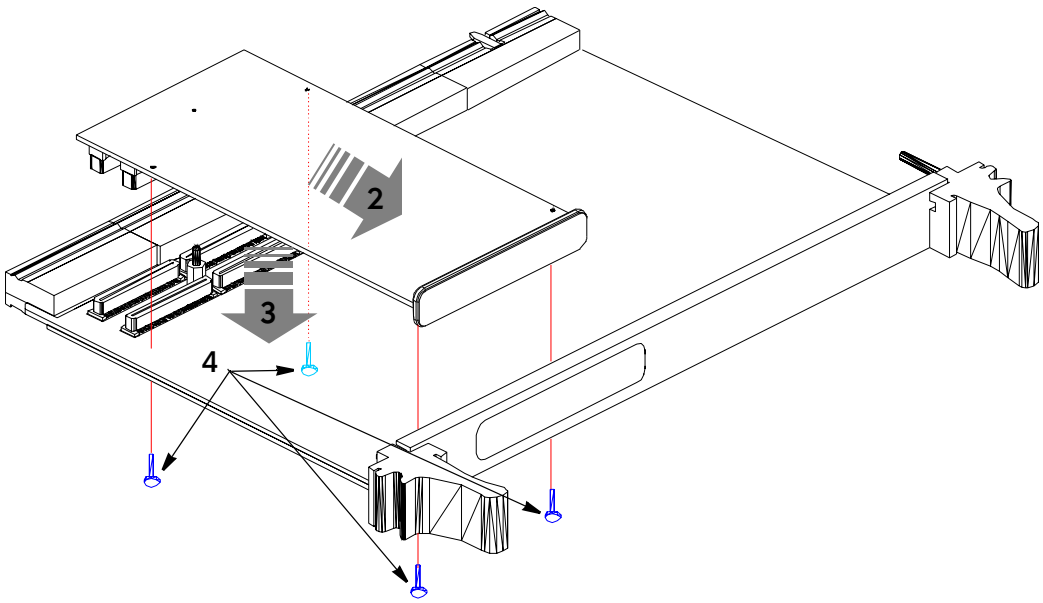
Before you begin

The EPC-6315 requires a PMC carrier.

Installing the EPC-6315 PMC on the carrier card

You install the EPC-6315 PMC on the carrier card as shown below.

Figure 2-1. Installing a PMC module



To install a PMC module:

1. Remove and save any blank faceplate from the PMC slot in the carrier card faceplate.
2. Position the PMC bezel through the PMC slot on the front panel.
3. Push the rear connectors into the carrier card.
4. Insert and tighten the screws on the back of the carrier card.

Using the 3-pin connector

The EPC-6315 includes a 3-pin connector that you can use to access some COM1 signals.

Before you begin, ensure that you have a null-modem cable that connects the 3-pin connector to your terminal.

You must construct this cable; RadiSys does not supply a cable for the 3-pin connector. For pinout information, see *3-pin connector* on page 76.

To use the 3-pin connector:

1. Attach the cable to the 3-pin connector and your terminal.
2. Start a terminal emulation program, such as Hyperterm or Telix, using these settings:

Baud rate:	115200
Parity:	None
Data bits:	8
Stop bits:	1
Flow control:	None

You can now access the BIOS setup program using the methods described in *Chapter 4, BIOS configuration*.

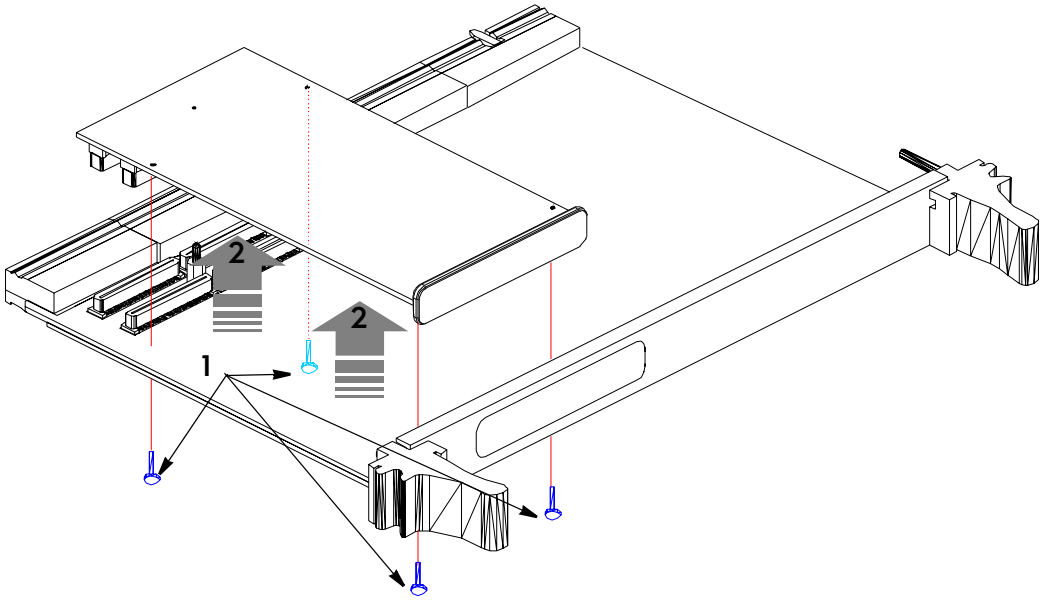
Maintaining and upgrading the EPC-6315

Occasionally you will want to perform maintenance or upgrades on the EPC-6315. When this occurs, you must remove the board from the carrier card, repair or install the desired option, then re-install the board on the carrier card. The following section describes how.

Disconnecting the EPC-6315 PMC from the carrier card

To separate the EPC-6315 from the carrier card:

Figure 2-2. Separating a PMC module from the carrier card



1. Remove screws on the back of the carrier card.
2. Pull the boards apart while keeping them parallel. Continue applying force until the connectors completely disengage.

After performing maintenance and/or upgrades, replace the EPC-6315 as described in *Installing the EPC-6315 PMC on the carrier card* on page 8.

3 Operating System Installation

This document explains how to install Linux and VxWorks operating Ssstems on the EPC-6315.

- For MV Linux LSPs, contact MontaVista at this URL:
  http://www.mvista.com
- For VxWorks BSPs, contact RadiSys or WindRiver
  http://www.windriver.com
  http://www.radisys.com

For information about... Go to this page...

Installing Red Hat Linux

You can install Red Hat using either of these methods:

- Install Red Hat on a separate computer..
- Install Red Hat over the serial port.

The following sections describe how.

Installing Red Hat on a separate computer

To install Red Hat, use a separate computer with a VGA card and prepare a hard drive for transfer to the EPC-6315:

1. Install a hard drive and CD-ROM drive in a PC with a VGA card. Ensure that the hard drive is the master on the primary cable.
2. Power on the system, insert the Red Hat bootable CD, and install Linux with the configuration you desire.
3. Reboot the system and log in at the Linux command prompt as “root”.

4. Configure Linux for serial redirection. Using any editor, change these files:

File	Instructions
/etc/inittab	1. Change the first TTY configuration line to read: `1: 2345:respawn:/sbin/mingetty ttyS0 115200 vt100` 2. Comment out the remaining TTY configuration lines. 3. Save your changes.
/etc/securetty	1. Add this line at the bottom of the file: `ttyS0` This file lists TTYs that allow logins. Adding the above line allows you to log in as root over the serial port. 2. Save your changes.

/etc/lilo.conf	1. In your kernel entry, add a kernel "append" parameter similar to this example:
	`image="/boot/vmlinuz-2.4.7-10"`
	`label="linux"`
	`read-only`
	`root="/dev/hda1"`
	`append = "console=ttyS0,115200n8"`
	Adding this parameter to the kernel instructs it to redirect kernel messages to the serial port.
	2. Save your changes.

5. Write changes to the master boot record by entering this command at the command prompt:

   ```
   lilo
   ```

6. Shut down the system.
7. Transfer the hard drive to the EPC-6315.
8. Boot the EPC-6315.

You can now log in over the serial port as root.

Installing Red Hat 7.3 or later over the serial port

Red Hat 7.3 already contains the correct TTY settings. This allows you to install Linux on the EPC-6315 without transferring the hard drive from another system. To install Red Hat 7.3 over the serial port:

1. Attach a hard drive and CD on an IDE cable, setting the hard drive to master and the CDROM to slave.
2. Power on the EPC-6315 system and immediately insert the Red Hat bootable CD-ROM.
3. Modify the BIOS settings to boot the EPC-6315 from the CD-ROM:
   A. Press F2 to enter the BIOS Setup program (see page 23).
   B. Make the CD-ROM the first device the EPC-6315 tries to boot from by moving the CD-ROM to the top of the list in the Boot menu (see page 46).

C. Change the console and terminal baud rates to 9600.

D. Press F10 to save your changes, then reboot.

The system boots over the serial port at 9600 bps, then displays the `boot:` prompt.

4. Enter this command:

```
linux console=ttyS0,9600n8
```

The serial port displays kernel messages.

5. Follow the instructions, configuring Linux to your liking. When prompted for kernel parameters, enter:

```
console=ttyS0,9600n8
```

Finish the installation and reboot the system. The serial port displays a login prompt at 9600 bps.

6. Log in as root.

7. To change the console baud rate to 115200, edit these files:

File	Instructions
/etc/inittab	1. Change the first TTY configuration line to read: `1: 2345:respawn:/sbin/mingetty ttyS0 115200 vt100` 2. Comment out the remaining TTY configuration lines. 3. Save your changes.

/etc/lilo.conf	1. In your kernel entry, add a kernel "append" parameter similar to this example:
	`image="/boot/vmlinuz-2.4.7-10"`
	`label="linux"`
	`read-only`
	`root="/dev/hda1"`
	`append = "console=ttyS0,115200n8"`
	2. Save your changes.

8. Write the changes to the master boot record by entering this command at the command prompt:

```
lilo
```

9. Reboot the system.

10. Change the baud rate:

A. During reboot, press F2 to enter the BIOS Setup program (see page 23).

B. Change the console and terminal baud rates to 115200 bps.

C. Press F10 to save each change.

The system boots over the serial port at 115200 bps, then displays the Linums login prompt.

Installing MontaVista Linux

This section explains how to network boot MontaVista Linux from the RadiSys-supplied LSP.

Configure the host to boot EPC-6315 over the network

The following sections provide instructions on how to configure the different components of the host system. These instructions are for only Linux hosts running Red Hat 7.3 or later.

Extract the kernel source and filesystem

1. Obtain the MontaVista Linux host tools from MontaVista (www.mvista.com).
2. Install the tools according to the host tools instructions. When the installation prompts you to install an LSP, choose any LSP based on an Intel Pentium III processor.
3. Extract kernel source files from the RadiSys-supplied LSP archive to a work area.

Configure DHCP

Ensure that the DHCP server is configured correctly. An incorrect configuration may cause problems for other machines on your network.

To configure DHCP as root:

1. Make sure a DHCP server is installed and that the following file exists:

Version	Filename
Red Hat 7.x	`/var/lib/dhcp/dhcpd.leases`

If the file does not exist, create an empty one using the Unix touch command:

Operating system	Command
Red Hat 7.x	`touch /var/lib/dhcp/dhcpd.leases`

2. Edit the DHCP daemon configuration file:
   A. Add the following configuration into your /etc/dhcpd.conf file:

```
allow bootp;
allow booting;
subnet SubAddress netmask NetAddress {
default-lease-time 1209600; # two weeks
max-lease-time 31557600; # one year
group {
    next-server TFTPAddress;
    option routers Gateway;
    host Target {
        hardware ethernet MACAddress;
        fixed-address IPAddress;
        option root-path "/opt/mvlcge/devkit/x86/pentium3/target";
        filename "bzImage.nb.mba";
        }
```

```
    }
}
```

B. Change the value of these parameters:

SubAddress The subnet address, consisting of four numbers from 0–255 separated by dots (periods).

NetAddress The netmask address, consisting of four numbers from 0–255 separated by dots (periods).

TFTPAddress The TFTP server address, consisting of four numbers from 0–255 separated by dots (periods).

Gateway The router or gateway address, consisting of four numbers from 0–255 separated by dots (periods).

Target The target name, consisting of three sections separated by dots (periods). For example:

```
test1.mvista.com
```

This name must be consistent with the host name used for DNS or host file look-up.

MACAddress The target MAC (Ethernet) address, consisting of six 2-digit numbers separated by colons:

```
xx:xx:xx:xx:xx:xx
```

The MAC address typically looks like this:

```
00:00:50:xx:xx:xx
```

IPAddress The target's IP address, consisting of four numbers from 0–255 separated by dots (periods).

3. Restart dhcpd by entering this command:

```
/etc/rc.d/init.d/dhcpd restart
```

The DHCP daemon is required to service BOOTP requests when booting the target. To run the DHCP daemon (on the host) on every boot, enter this command:

```
chkconfig dhcpd on
```

Use caution when running this command on a corporate network. Your DHCP server may interfere with the corporate DHCP server.

DHCP is now configured.

Configure TFTP

To configure TFTP, follow the instructions for the host you are using. The following instructions use the version of TFTP distributed with CGE.

Some host distributions do not have the most recent version of TFTP and some versions of TFTP do not work correctly with CGE. For that reason, MontaVista Software distributes a version of TFTP with CGE, installed by default at /opt/mvlcge/host/bin.

Red Hat 7.x

To configure TFTP on a Red Hat 7.x host as root:

1. Create (or edit) the file /etc/xinetd.d/tftp. Use the following format:

```
#/etc/xinetd.d/tftp
service tftp
{
    socket_type = dgram
    wait = yes
    user = root
    log_on_success += USERID
    log_on_failure += USERID
    server = /opt/mvlcge/host/bin/in.tftpd
    server_args = -r blksize /tftpboot
    disable = no
    protocol = udp
}
```

2. Ensure that the /tftpboot directory exists. To create the directory, enter this command:

```
mkdir /tftpboot
```

3. Have xinetd re-read its configuration file by entering this command:

```
/etc/rc.d/init.d/xinetd restart
```

4. Stop any any TFTP daemons that have not timed out by entering this command:

```
killall in.tftpd
```

Configure NFS

To configure NFS as root:

1. Add this line in /etc/exports:

```
/opt/mvlcge/devkit/x86/pentium3/target *(rw,no_root_squash,no_all_squash)
```

2. Stop, then start, the NFS daemon by entering these command:

```
/etc/rc.d/init.d/nfs stop
/etc/rc.d/init.d/nfs start
```

3. Set the NFS daemon to run during every boot by entering this command:

```
/sbin/chkconfig nfs on
```

4. Synchronize the NFS daemon by entering this command:

```
/usr/sbin/exportfs -ra
```

NFS is now configured.

Network boot the kernel

To network boot a kernel on the EPC-6315:

1. Change to the working folder (directory) where you placed the kernel sources.
2. Build the kernel by entering these commands:

```
make clean; make dep; make bzImage
```

3. Apply network boot headers to the kernel image by copying bzImage to /tftpboot.
4. Change the boot device:
   A. Attach:
      - An Ethernet cable to the EPC-6315 that allows access to your DHCP server.
      - A null modem cable from the EPC-6315 to a PC serial port.
   B. Open a terminal, such as minicom, and set the communications parameters to:

      Baud rate: 115200
      Parity: None
      Data bits: 8
      Stop bits: 1
      Flow control: None

   C. Power-on the EPC-6315.
   D. Enter the BIOS and set the first boot device as UNDI (on-board Ethernet). Press F10 to save and reboot. The kernel boots over the network and displays on the serial port.
5. Log in as root.

Install MontaVista Linux to a hard drive

Creating a bootable hard drive or CompactFlash requires that you network boot a kernel and NFS a filesystem, as described in the previous section. You then attach a bootable media device, prepare a filesystem on it, and copy the filesystem over NFS.

1. Prepare the bootable media:
   A. Attach a CompactFlash into the front panel slot or attach an IDE hard drive to the IDE connector on your baseboard. Be sure that the hard drive is set up as the master.
   B. Network boot the system over the serial port at 115200 bps.
   C. Run fdisk:
      i. Create partitions on the drive by entering this command:

         ```
         fdisk /dev/hda
         ```

      ii. Create at least one partition to use as /root.
      iii. Tag the partition with ID 83, using the `t` command.
      iv. Mark it bootable by using the `a` command.
      v. Save your changes by entering `w`.

For more information about fdisk, see the HOWTOs on using fdisk, available on the web.

You can find out more about fdisk at www.redhat.com. To locate the utility, search for fdisk on the site.

2. Prepare a filesystem:
   A. Create a filesystem by entering this command:

      ```
      mkfs-ext2 /dev/hda1
      ```

   B. Mount the filesystem to /mnt by entering this command:

      ```
      mount /dev/hda1 /mnt
      ```

   C. Copy the filesystem from NFS to the mount point /mnt by entering these commands:

      ```
      cp -aR /bin /mnt
      cp -aR /boot /mnt
      cp -aR /dev /mnt
      cp -aR /etc /mnt
      cp -aR /home /mnt
      cp -aR /lib /mnt
      cp -aR /opt /mnt
      cp -aR /root /mnt
      cp -aR /sbin /mnt
      cp -aR /tmp /mnt
      cp -aR /usr /mnt
      cp -aR /var /mnt
      mkdir /mnt/mnt
      mkdir /mnt/proc
      ```

3. On your host, copy the bzImage kernel you created (in step 2 of *Network boot the kernel* on page 16) to /root. On the EPC-6315 terminal, copy this image to /mnt/boot.
4. Change the current /root to the mounted drive by entering this command:

   ```
   chroot /mnt
   ```

5. Configure Linux for serial redirection. Using any editor, change this file:

File	Instructions

/etc/lilo.conf	1. Revise the file similar to this example, paying particular attention to the tty settings:
	`timeout="50"`
	`default="MVL CGE 2.1"`
	`boot=/dev/hda`
	`map=/boot/map`
	`install=/boot/boot.b`
	`append="console=ttyS0,115200n8"`
	`lba32`
	`image="/boot/bzImage"`
	`label="MVL CGE 2.1"`
	`read-only`
	`root=/dev/hda1`
	2. Save your changes.

6. Write the changes to the master boot record by entering this command at the command prompt:

   ```
   lilo
   ```

7. Reboot the system.

   A. Press F2 to enter the BIOS Setup program (see page 23).

   B. Change the first boot device to be the bootable drive.

   C. Press F10 to save and reboot.

You should now boot from CompactFlash or the hard drive with a serial console.

Installing VxWorks

This section explains how to install VxWorks on a blank CompactFlash or hard drive.

Requirements

To install a VxWorks BSP on an EPC-6315 you will need:

- The EPC-6315 VxWorks BSP from RadiSys. You can request it from RadiSys by sending email to support@radisys.com.
- A DOS boot disk with fdisk and format utilities.
- Two DOS-formatted floppy diskettes.
- A 10MB or greater CompactFlash or hard drive.
- A CF-to-IDE (standard hard drive connector) adapter (needed only if you plan to install VxWorks on CompactFlash).

Installation

1. Install the BSP:
   A. Obtain the RadiSys EPC-6315 VxWorks BSP from RadiSys. You can request it from support@radisys.com.
   B. Install the BSP by extracting the archive and running setup.exe.
2. Build projects:
   A. In the Tornado environment, create a project based on the EPC6315 BSP.
   B. Build bootrom_uncmp and vxWorks.st.

   For more information about creating and building files, see your VxWorks documentation.
3. Create a boot disk with the VxWorks bootloader:
   A. Insert a formatted floppy into your disk drive.
   B. In a DOS box, change to the directory where bootrom_uncmp resides.
   C. Create a bootable floppy by entering this command:

      ```
      mkboot a: bootrom_uncmp
      ```

   D. Copy the vxsys.com file to the floppy diskette. Typically, this file resides at

      ```
      c:\tornado\host\x86-win32\bin\
      ```

   E. Copy the VxWorks.st image to the boot floppy by entering:

      ```
      copy vxWorks.st a:
      ```

      If this file does not fit on the boot floppy, copy vxWorks.st to a different floppy.
   F. Label this as the EPC-6315 bootdisk.
4. Prepare the device to be the boot device:
   A. On a separate computer, install the HD or CF card as drive C (i.e., Master drive on primary IDE cable for a HD, to install to CF a CF-to-IDE adapter must be used). The HD or CF must be the first drive and, when formatted, be recognized in DOS as drive C.
   B. Boot the PC from a DOS boot disk.
   C. Run fdisk and create a bootable FAT filesystem and restart the system.
   D. When the DOS prompt displays, enter this command:

      ```
      format c:
      ```

   E. Remove the DOS disk and insert the VxWorks bootdisk.

5. Make a VxWorks-bootable hard drive or CompactFlash by entering these commands:

Command	Description
`vxsys c:`	Installs the master boot record and initial bootloader
`copy bootrom.sys c:`	Copies the VxWorks bootloader to the drive.
`copy vxWorks.st c:`	Copies VxWorks image to the drive.

6. Install the device in the system:
   A. Power down the system and remove the hard drive or CompactFlash card.
   B. Transfer the drive to the EPC-6315 system.
7. Start VxWorks:
   A. Boot the EPC-6315 system.

The default is to boot from "ata0", which is the CompactFlash card or master hard drive.

When the bootloader (bootrom_uncmp) runs, a countdown displays.

   B. Press a key to display a prompt, then enter `c` to configure your system. Set IP information to the values you desire.

To have VxWorks automatically initialize the on-board Ethernet, enter `fei` into the "other" field.

After you enter the parameters, the configuration is saved automatically to flash.

   C. Boot VxWorks by entering `@`.

4 BIOS configuration

The EPC-6315 uses the Phoenix NuBIOS to configure and select various system options. This chapter details the various menus and sub-menus used to configure the system. This chapter is written as though you are setting up each field in sequence and for the first time. Your system may be correctly pre-configured and require very little setup.

To revert to the original BIOS settings, select Load Setup Defaults from the *Exit menu* on page 48. This restores the original BIOS settings.

You may see some error messages during the execution of the BIOS initialization sequence. If errors occur during the POST (Power-On Self-Test), the BIOS displays the error on the appropriate line of the screen display and, depending on how your system is configured, either pauses or tries to continue. For information about error messages, see *Appendix D, Error messages*.

Pressing the Escape key during POST displays the Boot-First pop-up menu after POST completes. You can use this menu to override, for only this boot, the boot options. This menu includes the same options as the Boot Menu's top level. For information about the options, see *Boot menu* on page 46.

BIOS setup screens

The EPC-6315's BIOS includes a setup program that displays and modifies the system configuration. The EPC-6315's nonvolatile CMOS RAM stores configuration information, and the BIOS uses it to initialize the EPC-6315 hardware.

You can enter the BIOS Setup only during the system reset process, following a power-up, front panel reset, or equivalent. To enter Setup, press the F2 key when prompted.

To view BIOS setup screens, the EPC-6315 must be attached to a terminal. For information about attaching to a terminal, see *Using the 3-pin connector* on page 9.

Menu map

You set up the BIOS by making selections from the menus shown in the next table.

When reading this file online, you can immediately view information about any menu by placing the mouse cursor over menu name and clicking:

Menu	Sub-menu
Main Setup menu	Primary Master/Slave sub-menus
Advanced menu	PCI Configuration sub-menu PrPMC customizations sub-menu PCI/PNP ISA UMB Region Exclusion sub-menu PCI/PNP ISA IRQ Resource Exclusion sub-menu Cache Memory sub-menu Console Redirection sub-menu I/O Device Configuration sub-menu
Boot menu	None
Exit menu	CMOS Save & Restore sub-menu

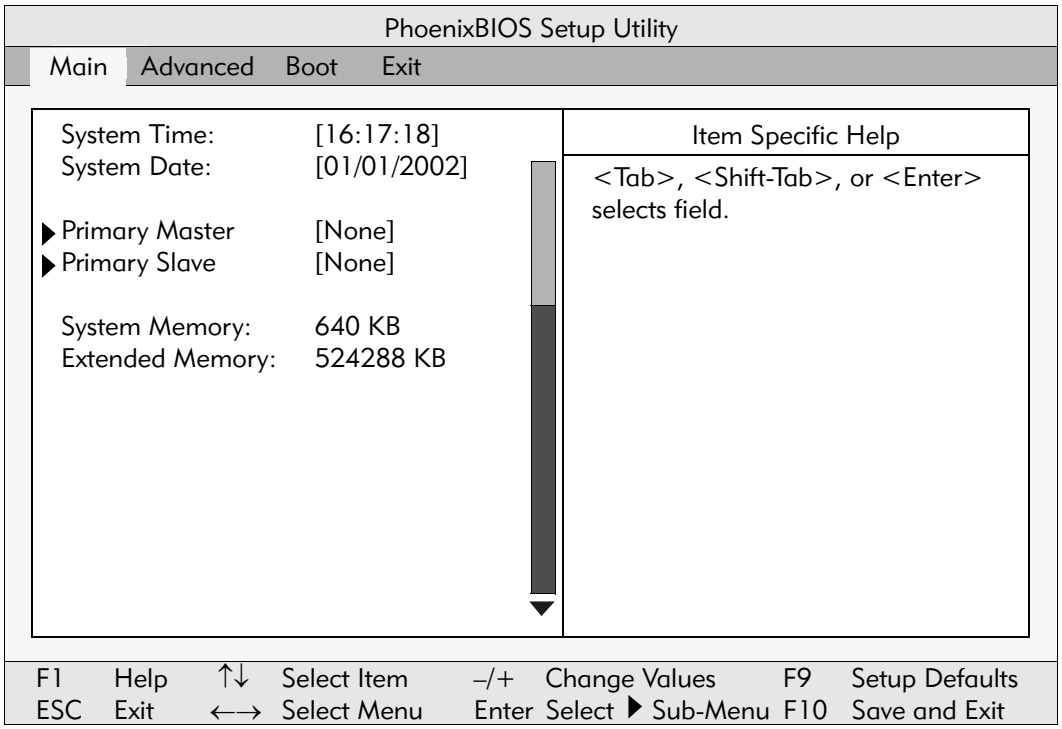
Navigation

To...	Do...
Display a menu	Press the left or right cursor (arrow) keys and press the Enter key. If you use the arrow keys to leave a menu and then return, your active field is always at the beginning of the menu.
Display a submenu (fields with a triangle at left)	Move the cursor to a field with a triangle and press the Enter key. If you select a sub-menu and then return to the main menu, the active field is that sub-menu heading.
Select a field	Press the up or down cursor (arrow) keys
Select an option	Do one of these: • Press the + and – keys to rotate through available options. • In certain numeric fields, simply enter the desired number.

The remainder of this chapter describes the fields in each menu and sub-menu. Additional help information is available in the help area on the Setup screen.

Main Setup menu

Figure 4-1. BIOS Main Setup menu



The far right menu in the menu bar is the Exit Menu. Use the options in the Exit menu to save your changes, re-load default BIOS settings, and so on. Press the ESC key to go immediately to the Exit Menu.

The fields in each menu and sub-menu are explained below. Additional help information is available in the help area on the BIOS setup screen.

Field	Description
System Time/System Date	Sets the system time and date. To change these values, go to each field and enter the desired value. Press the tab key to move from hour to minute to second, or from month to day to year. The default system time is 00:00; the default date is 01/01/1998.
Primary Master sub-menu	Displays a menu that you use to enter information for the master IDE drive connected to the primary IDE controller. For more information, see *Primary Master/Slave sub-menus* on page 27.
Primary Slave sub-menu	Displays a menu that you use to enter information for the slave IDE drive connected to the primary IDE controller.For more information, see *Primary Master/Slave sub-menus* on page 27.

Field	Description
Boot Options sub-menu	Displays a menu that you use to specify the PC's behavior during the boot process. For more information, see *Boot menu* on page 46.
System memory	Displays the amount of conventional memory (below 1MB). This field is not editable; no user interaction is required.
Extended memory	Displays the amount of extended memory (above 1MB). This field is not editable; no user interaction is required.

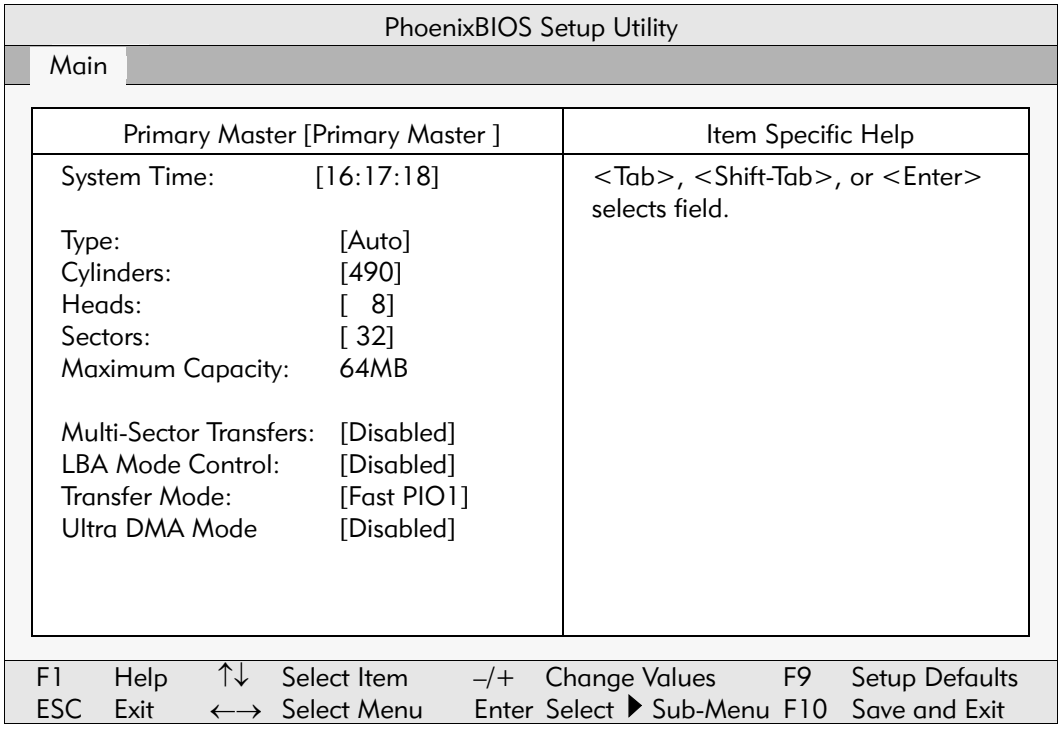
Primary Master/Slave sub-menus

There are two IDE adapter sub-menus for the primary hard disk controllers: a master and slave drive menu.

Access this screen to:

- See or reconfigure the detailed characteristics of the primary hard disk (select the IDE Adapter 0 Master item from the Main BIOS Setup).
- Set up new disks and allow the Setup program to determine the proper settings based on information on the disk. Note that the Setup program can detect these settings only on drives that comply with ANSI specifications.
- Set up existing (formatted) disks. Note that you must use the same parameters used when the disk originally was formatted. You must select an option for the Type field, then enter the specific cylinder, head, and sector information listed on the label attached to the drive at the factory.

Figure 4-2. Primary Master/Slave sub-menus



Field	Description
Type	Identifies the disk type. You can select one of these: • **Auto (default)**: Select this option when you want the POST to query the hard disk for its parameters whenever the POST runs. RadiSys recommends this option. **Note**: If you set a hard disk to "Auto", but no hard disk is actually present, the BIOS queries the (non-existent) hard disk until it times out, slightly increasing the duration of the POST. • **None**: Select this option if yours is not an IDE hard disk drive. • **User**: Select this option if you have an IDE disk but cannot employ the "Autotype" feature. Then enter the correct drive values for cylinders, heads, sectors/track, and write precompensation. • **ATAPI Removable**: Select this option if you have a removable disk drive. • **IDE Removable**: Provides support for high-capacity disks that can be formatted as floppy or hard disks. This option may be used for compact flash cards. • **CD-ROM**: Select this option if you have a CD-ROM drive. • **1–39**: Select this option to specify a pre-determined hard-disk drive type. These drive types, found in the FDPT (Fixed Disk Parameter Table), are seldom used. RadiSys recommends that you avoid using this option. **Note**: For disks not supplied, consult the product documentation. When finished, press the ESC key to return to the *Main Setup menu*.
Cylinders	Specifies the number of cylinders on this system. You can specify a number from 1 to 16. **Note**: This field displays only when the Type field contains a value of [User] or [1–39]. You can edit this field only when the Type field contains a value of [User].
Heads	Specifies the number of heads on this system. **Note**: This field displays only when the Type field contains a value of [User] or [1–39]. You can edit this field only when the Type field contains a value of [User].
Sectors	Specifies the number of sectors in each track on this system. **Note**: This field displays only when the Type field contains a value of [User] or [1–39]. You can edit this field only when the Type field contains a value of [User].

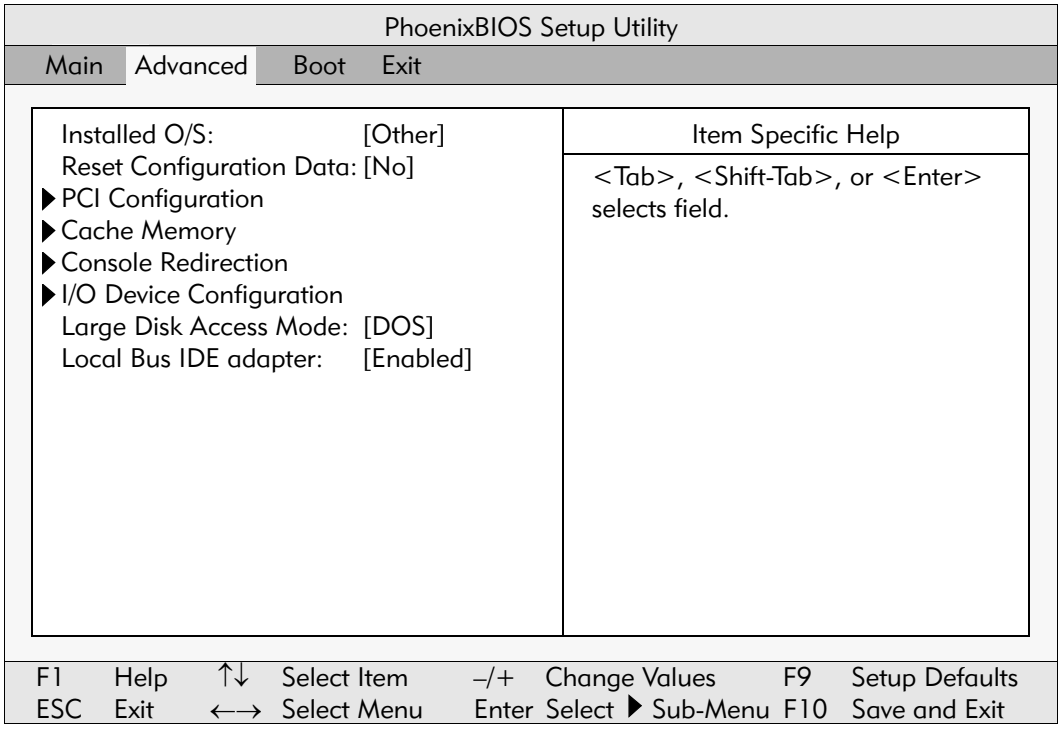
Field	Description
Multi-Sector Transfers	Allows the System BIOS to read ahead by the specified number of sectors during disk access. This has the effect of reading more data at once to reduce the absolute number of discrete disk reads performed by the operating system, which may increase system performance. You can select one of these: • Disabled (default if no drive is installed) • 2 Sectors • 4 Sectors • 8 Sectors • 16 Sectors (default if a drive is installed) **Note**: This field displays only when the Type field contains a value of [User] or [1–39]. Autotyping may change this value if the hard disk reports that it supports block accesses.
LBA Mode Control	Determines how the System BIOS references hard disk data. You can use this option only if both the hard disk being configured and the operating system support LBA (Logical Block Addressing). Autotyping may change this value if the hard disk reports that it supports LBA. You can select one of these: • **Disabled (default if no drive is installed)**: Reference hard disk data using the CHS (Cylinders/Heads/Sectors) method. • **Enabled (default if a drive is installed)**: Reference hard disk data as logical blocks. **Note**: This field displays only when the Type field contains a value of [None].

Field	Description
Transfer Mode	Selects the mode that the System BIOS uses to access the hard disk. You can select one of these: • Standard • Fast PIO 1 • Fast PIO 2 • Fast PIO 3 • Fast PIO 4 (default) • FPIO 3 / DMA 1 • FPIO 4 / DMA 2 Older hard disks only support "Standard". Newer hard disks adhering to "Fast ATA" or "Enhanced IDE" specifications may support the fast programmed I/O or DMA modes. Note that autotyping may change this value depending on the transfer modes that the hard disk reports it supports. The fast DMA modes take full advantage of the onboard bus mastering hard disk controller and should yield the highest performance when used in conjunction with multitasking operating systems that support it. **Note**: This field displays only when the Type field contains a value of [None].
Ultra DMA Mode	Selects the Ultra DMA Mode that the System BIOS uses to access the hard disk. You can select one of these: • Mode 2 (default) • Mode 1 • Mode 0 • Disabled **Note**: This field displays only when the Type field contains a value of [None]. Autotyping derives this value from information reported by the drive.

Advanced menu

This menu contains settings for integrated peripherals, memory shadow, cache, and large disk access mode. You access this menu by selecting Advanced from the Main BIOS Setup menu.

Figure 4-3. Advanced menu



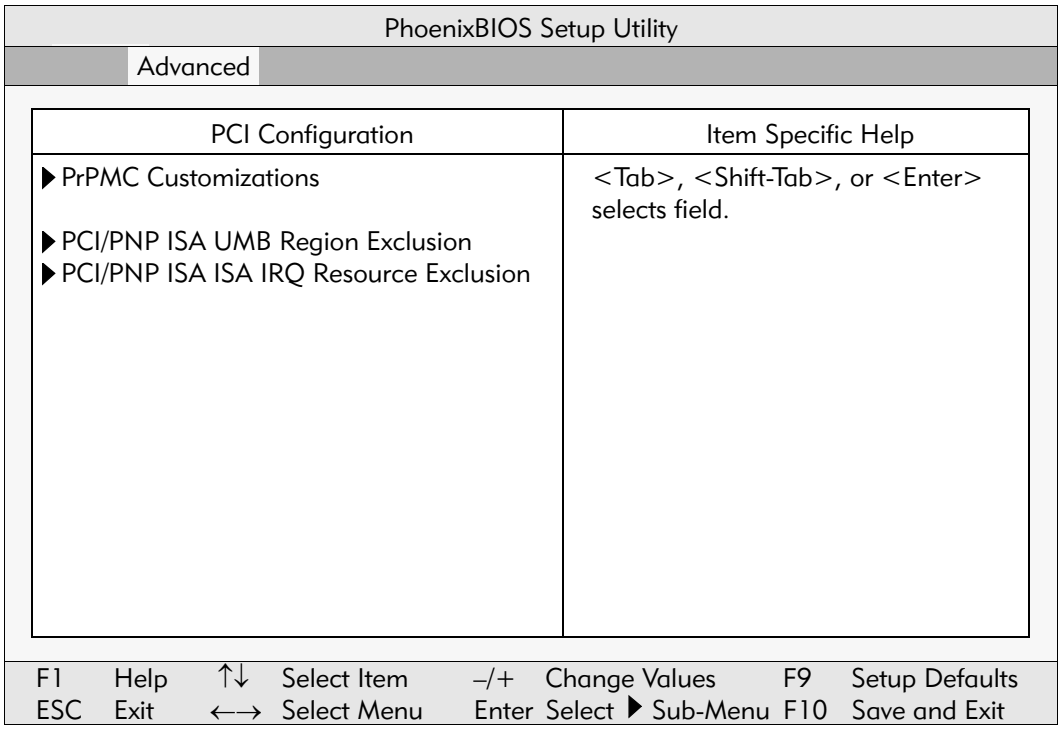
Field	Description
Installed OS	Identifies the OS you plan to use on this system. Identifying the OS determines how much initialization the BIOS performs. You can select one of these: • **Other (default)**: The Plug-and-Play BIOS completes PCI initialization. Select this option when you plan to use an OS other than Win95. • **Win95**: Only boot devices are initilized; the remainder of initialization is completed by the OS. Select this option when you plan to use Windows 95 as your OS. **Note**: Setting this to the incorrect value may produce unexpected results.

Field	Description
Reset Configuration Data	Determines whether to clear the Extended System Configuration Data (ESCD) block that resides in the Flash Boot Device (FBD). You can select one of these: • **No (default)**: Does not clear the ESCD block. • **Yes**: Clears the ESCD block. You must clear the block the first time a system is turned on or if the ESCD becomes corrupted. This option automatically resets to "No" after the block is cleared.
PCI Configuration sub-menu	Displays a menu that you use to configure PCI devices. For more information, see *PCI Configuration sub-menu* on page 33.
Cache Memory sub-menu	Displays a menu that you use to control the use of the CPU cache. For more information, see *Cache Memory sub-menu* on page 38.
Console Redirection sub-menu	Displays a menu that you use to redirect console output. For more information, see *Console Redirection sub-menu* on page 43.
I/O Device Configuration sub-menu	Displays a menu that you use to configure peripheral devices. For more information, see *I/O Device Configuration sub-menu* on page 45.
Large Disk Access Mode	Specifies whether MS-DOS systems can use hard disks up to 8GB (1024C x 255H x 63S) without special drivers or LBA. If the drive fails while installing new software, change this setting and try again. You can select one of these: • **DOS (default)**: Causes the System BIOS to perform cylinder/head translation if the drive is configured in Setup to have more than 1024 cylinders. Select this option if your system uses a drive larger than 528 MB and runs DOS or MS-DOS†. • **Other**: Select this option if your system uses a drive larger than 528 MB and runs an OS other than DOS.
Local Bus IDE Adapter	Configures the integrated local bus IDE adapter. You can select one of these: • Enabled (default) • Disabled

PCI Configuration sub-menu

Use the options in this sub-menu to control the exclusion of the UMB region for PCI or ISA and the exclusion of the IRQs for PCI or ISA.

Figure 4-4. PCI Configuration sub-menu

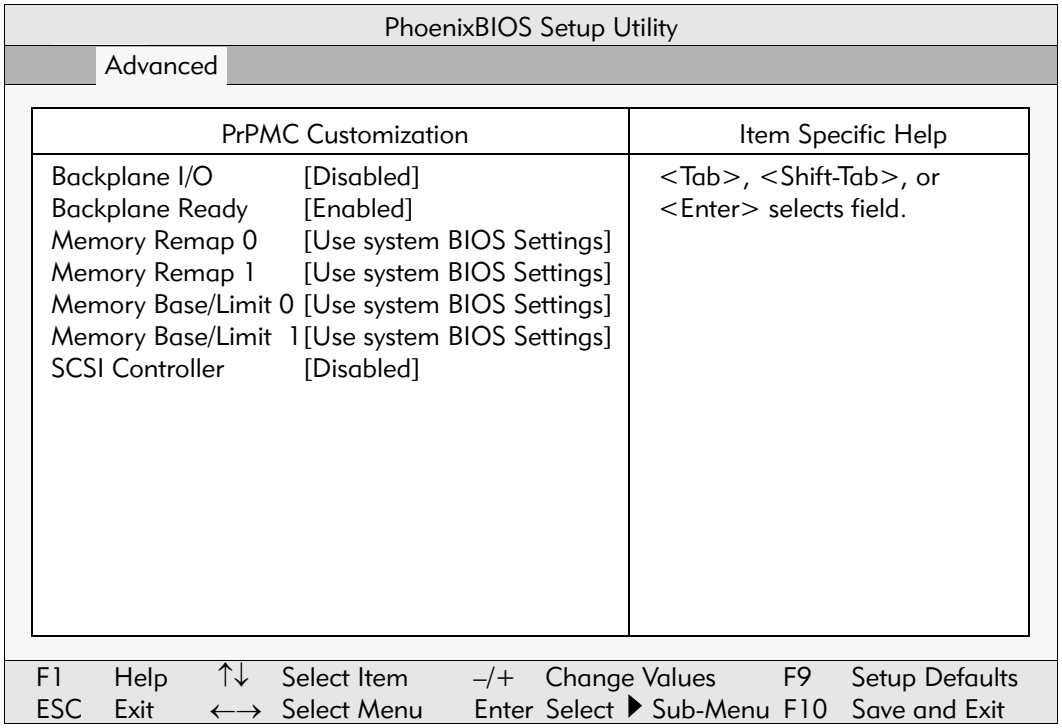


Field	Description
PrPMC Customizations sub-menu	Displays a menu that you use to customize PrPMC options. For more information, see *PrPMC customizations sub-menu* on page 34.
PCI/PNP ISA UMB Region Exclusion	Displays a menu that you use to control the exclusion of PCI and ISA Upper Memory Block (UMB) regions. For more information, see *PCI/PNP ISA UMB Region Exclusion sub-menu* on page 36.
PCI/PNP ISA ISA IRQ Resource Exclusion	Displays a menu that you use to control the exclusion of PCI and ISA interrupt resources. For more information, see *PCI/PNP ISA IRQ Resource Exclusion sub-menu* on page 37.

PrPMC customizations sub-menu

Options in this menu customize PrPMC options.

Figure 4-5. PrPMC customizations sub-menu



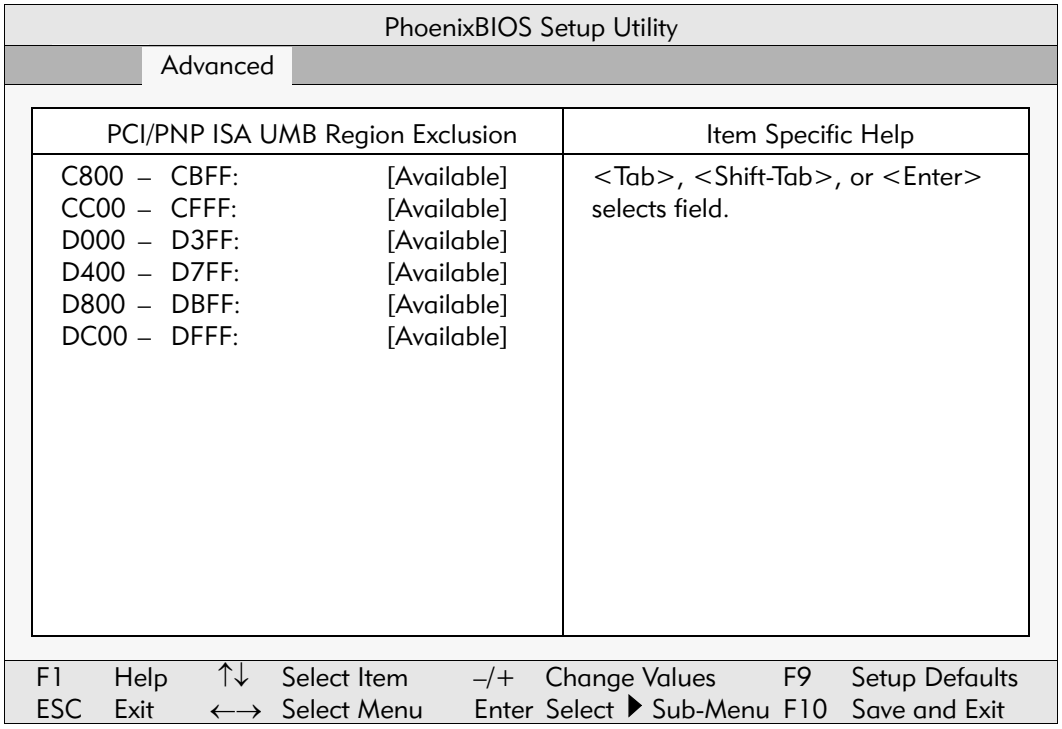
Field	Description
Backplane I/O	Determines how the backplane implements I/O. You can select one of these: • **Disabled (default)**: The local PCI bus services all I/O accesses. • **Enabled**: I/O addresses pass through to the backplane PCI bus.
Backplane Ready	Determines how resources are assigned during boot. You can select one of these: • **Enabled (default)**: Selecting this option sets the Backplane Ready bit after resources are assigned. • **Disabled**: Selecting this option prevents the Backplane Ready bit being set by the System BIOS.
Memory Remap *n*	Maps local DRAM into backplane PCI space. You can select one of these: • Use system BIOS settings (default) • 0 • 1 MB • 16 MB • 256 MB • 512 MB

Field	Description
Memory Base/Limit *n*	Forces memory/base and limit registers. You can select one of these: • Use system BIOS settings (default) • F100F000 • F300F200 • F500F400 • F700F600 • F900F800 • FB00FA00 • F000A000
SCSI Controller	Determines the state of the SCSI controller on the carrier card. You can select one of these: • **Disabled (default)**: Disables the controller. • **Enabled**: Enables the controller. **Note**: If the card does not have a SCSI controller, this option has no effect.

PCI/PNP ISA UMB Region Exclusion sub-menu

The PCI/PNP ISA UMB Region Exclusion Sub-Menu controls the exclusion of PCI and ISA UMB regions.

Figure 4-6. PCI/PNP ISA UMB Region Exclusion sub-menu

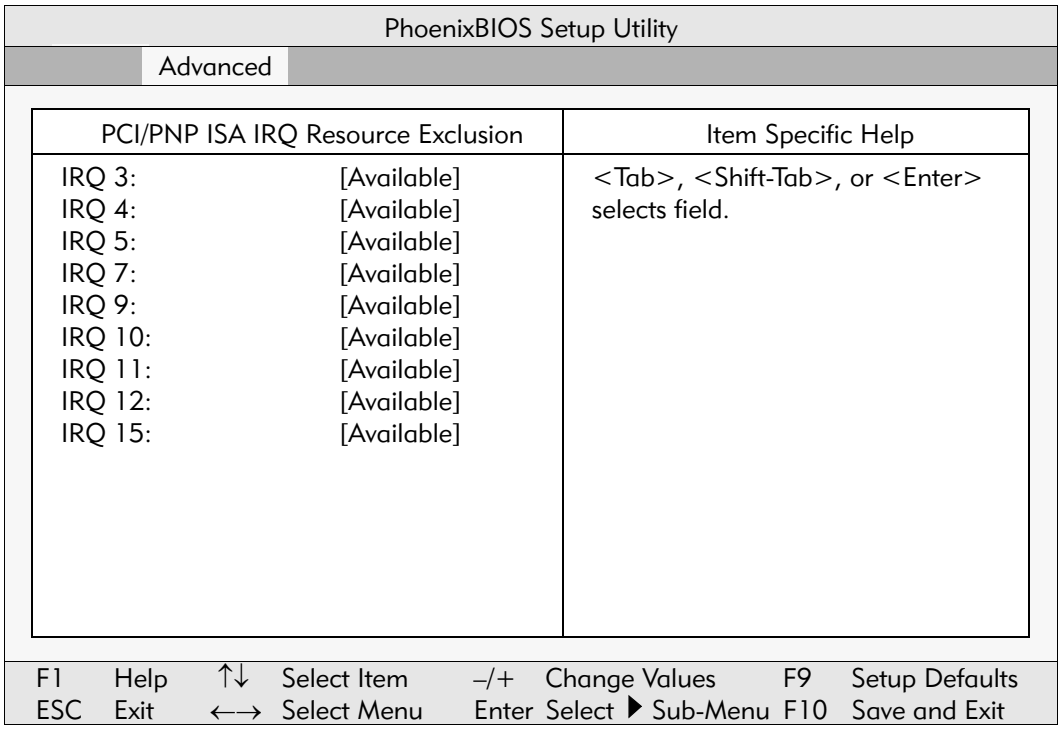


Field	Description
Memory Regions	Determines the use of each UMB region. You can select one of these: • **Available (default)**: Makes the regions available for PCI use. • **Reserved**: Reserves the specified block of upper memory regions for ISA use.

PCI/PNP ISA IRQ Resource Exclusion sub-menu

The PCI/PNP ISA IRQ Resource Exclusion Sub-Menu controls the exclusion of PCI and ISA interrupt regions.

Figure 4-7. PCI/PNP ISA IRQ Resource Exclusion sub-menu

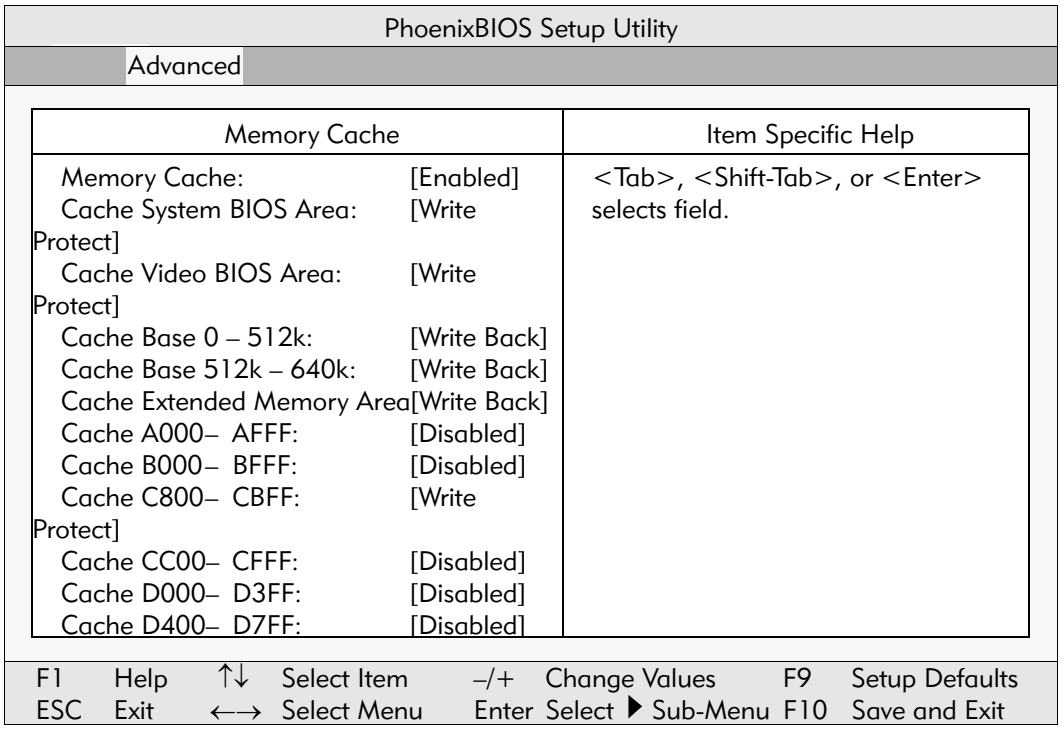


Field	Description
Interrupts	Determines the use of each interrupt. You can select one of these: • **Available (default for IRQs 3, 4, 5, 9, and 12)**: Makes the ISA IRQ available for PCI use. • **Reserved (default for IRQs 7, 10, and 11)**: Reserves the interrupt for ISA use. Select this option if the IRQ is required by an on-board ISA peripheral or an ISA card. **Note**: The IRQ10 interrupt is reserved for soft reset.

Cache Memory sub-menu

The options in this sub-menu control the cacheability of certain memory regions and also the settings of the Level 2 (L2) cache.

Figure 4-8. Cache Memory sub-menu



Field	Description
Memory Cache	Determines whether to use L2 memory caching. You can select one of these: • **Enabled (default)**: L2 memory caching occurs. • **Disabled**: L2 memory caching does not occur.
Cache System BIOS Area	Determines whether the System BIOS is cached in DRAM. You can select one of these: • **Write Protect (default)**: caches the System BIOS in the F0000h through FFFFFh DRAM area • **uncached**: Does not cache the system BIOS.
Cache Video BIOS Area	Determines whether the VGA BIOS is cached in DRAM. You can select one of these: • **Write Protect (default)**: caches the VGA BIOS in the C0000h through C7FFFh DRAM region. • **uncached**: Does not cache the VGA BIOS.

Field	Description
Cache Base 0–512k Cache Base 512–640k	Determines how the system caches base memory in the specified area: You can select one of these: • **Write Back (default)**: Writes and reads to and from system memory are cached, then written to system memory when you perform a write-back operation. Select this option to reduce bus traffic by eliminating unnecessary writes to system memory. This option provides the best performance, but requires that all devices that access system memory on the system bus be able to snoop memory accesses to ensure system memory and cache coherency. • **Write Through**: Writes and reads to and from system memory are cached. Select this option for frame buffers or when there are devices on the system bus that access system memory, but do not perform snooping of memory accesses. • **Write Protect**: Reads come from cache lines when possible, and read misses cause cache fills. Writes are propagated to the system bus and cause corresponding cache lines on all processors on the bus to be invalidated. Speculative reads are allowed. • **uncached**: The system does not cache memory.
Cache Extended Memory Area	Determines how the system caches extended memory. You can select one of these: • **Write Back (default)**: Writes and reads to and from system memory are cached, then written to system memory when you perform a write-back operation. Select this option to reduce bus traffic by eliminating unnecessary writes to system memory. This option provides the best performance, but requires that all devices that access system memory on the system bus be able to snoop memory accesses to ensure system memory and cache coherency. • **Write Through**: Writes and reads to and from system memory are cached. Select this option for frame buffers or when there are devices on the system bus that access system memory, but do not perform snooping of memory accesses. • **Write Protect**: Reads come from cache lines when possible, and read misses cause cache fills. Writes are propagated to the system bus and cause corresponding cache lines on all processors on the bus to be invalidated. Speculative reads are allowed. • **uncached**: The system does not cache memory.

Field	Description
Cache Memory Regions: A000–AFFF B000–BFFF	Determines how the system deals with specified memory blocks or shadow[1] memory. You can select one of these: • **Disabled (default)**: The system does not cache memory. • **USWC Caching**: System memory locations are not cached (as with uncacheable memory) and coherency is not enforced by the processor's bus coherency protocol. Speculative reads are allowed. Writes may be delayed and combined in the write buffer to reduce memory accesses. Select this option for video frame buffers, where the write order is unimportant as long as the writes update memory so they can be seen on the graphics display. • **Write Back**: Writes and reads to and from system memory are cached, then written to system memory when you perform a write-back operation. Select this option to reduce bus traffic by eliminating unnecessary writes to system memory. This option provides the best performance, but requires that all devices that access system memory on the system bus be able to snoop memory accesses to ensure system memory and cache coherency. • **Write Through**: Writes and reads to and from system memory are cached. Select this option for frame buffers or when there are devices on the system bus that access system memory, but do not perform snooping of memory accesses. • **Write Protect**: Reads come from cache lines when possible, and read misses cause cache fills. Writes propagate to the system bus and cause corresponding cache lines on all processors on the bus to be invalidated. Speculative reads are allowed. When BIOS extensions are present in these regions, enabling caching for that region increases performance

Field	Description
Cache Memory Regions: C800–CBFF CC00–CFFF D000–D3FF D400–D7FF D800–DBFF DC00–DFFF	Memory regions. Determines how the system deals with specified memory blocks or shadow[1] memory. You can select one of these: • **Disabled (default)**: The system does not cache memory. • **Write Back**: Writes and reads to and from system memory are cached, then written to system memory when you perform a write-back operation. Select this option to reduce bus traffic by eliminating unnecessary writes to system memory. This option provides the best performance, but requires that all devices that access system memory on the system bus be able to snoop memory accesses to ensure system memory and cache coherency. • **Write Through**: Writes and reads to and from system memory are cached. Select this option for frame buffers or when there are devices on the system bus that access system memory, but do not perform snooping of memory accesses. • **Write Protect**: Reads come from cache lines when possible, and read misses cause cache fills. Writes propagate to the system bus and cause corresponding cache lines on all processors on the bus to be invalidated. Speculative reads are allowed. When BIOS extensions are present in these regions, enabling caching for that region increases performance

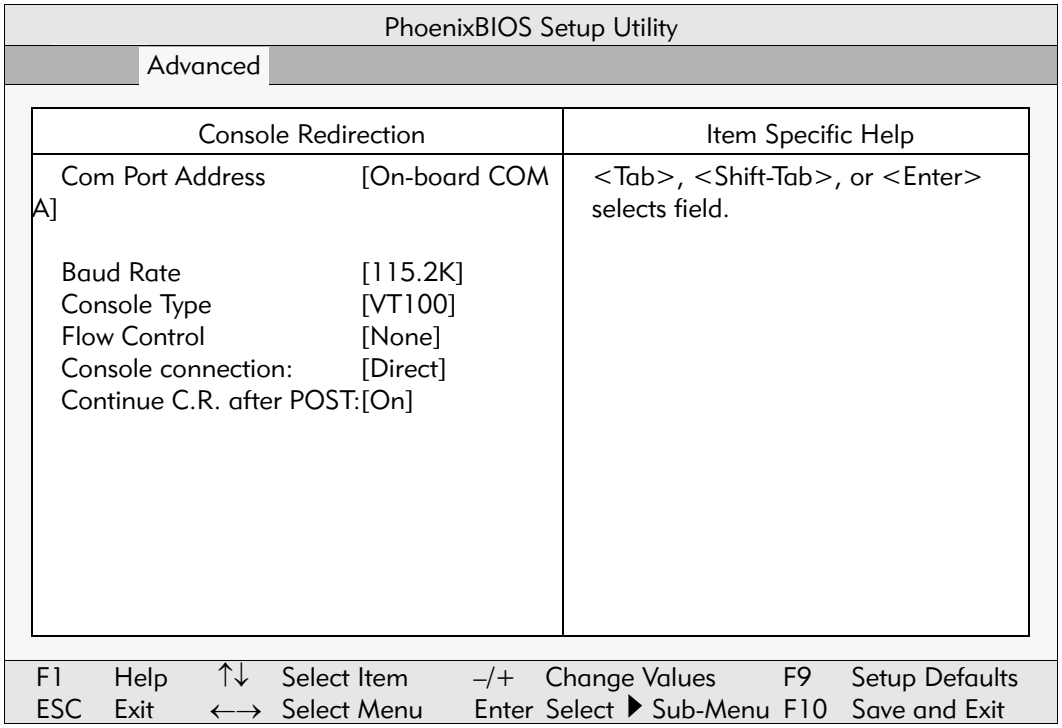
Field	Description
Cache Memory Regions: E000–E3FF E400–E7FF E800–EBFF EC00–EFFF	Memory used in the E0000h–EFFFFh DRAM region. Determines how the system deals with specified memory blocks or shadow[1] memory. You can select one of these: • **Disabled (default)**: The system does not cache memory. • **Write Back**: Writes and reads to and from system memory are cached, then written to system memory when you perform a write-back operation. • Select this option to reduce bus traffic by eliminating unnecessary writes to system memory. • This option provides the best performance, but requires that all devices that access system memory on the system bus be able to snoop memory accesses to ensure system memory and cache coherency. • **Write Through**: Writes and reads to and from system memory are cached. • Select this option for frame buffers or when there are devices on the system bus that access system memory, but do not perform snooping of memory accesses. • **Write Protect**: Reads come from cache lines when possible, and read misses cause cache fills. Writes propagate to the system bus and cause corresponding cache lines on all processors on the bus to be invalidated. Speculative reads are allowed. When BIOS extensions are present in these regions, enabling caching for that region increases performance

[1] *Shadowing* refers to the technique of copying BIOS extensions from ROM into DRAM and accessing them from DRAM. This allows the CPU to access the BIOS extensions much more quickly and generally increases system performance if many calls to the BIOS extensions are made.

Console Redirection sub-menu

Options in this menu configure console redirection.

Figure 4-9. Console Redirection sub-menu



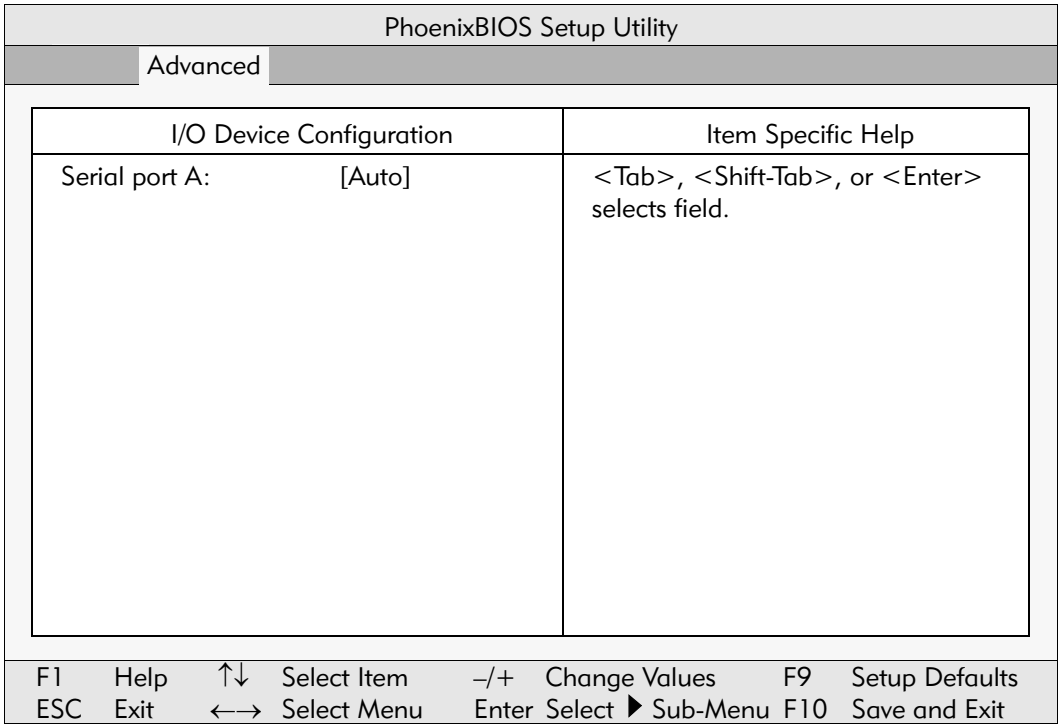
Field	Description
Com Port Address	Specifies the serial port to use for console redirection. You can select one of these: • **On-board COM A (default)**: The system uses COM A for redireton. • **Disabled**: The system does not redirect input.
Baud Rate	Specifies the baud rate at which the COM port operates. You can select one of these: • 600 • 1200 • 2400 • 4800 • 9600 • 19.2K • 38.4K • 115.2K (default)
Console Type	Identifies the console type. You can select one of these: • VT100 (default) • PC ANSI
Flow Control	Specifies flow control. You can select one of these: • None (default) • CTS/RTS • XON/XOFF

Field	Description
Console connection	Specifies how the console connects to the system. You can select one of these: • **Direct (default)**: Connects the console directly to the system. • **Via modem**: Connects the console to the system via a modem.
Continue C.R. after POST	Determines whether console redirection occurs after BIOS hands off to the OS. You can select one of these: • **On (default)**: Console redirection continues as and after the OS loads. • **Off**: Console redirection stops when the OS starts to load.

I/O Device Configuration sub-menu

Use the options in this sub-menu to configure the onboard serial disk controller.

Figure 4-10. I/O Device Configuration sub-menu



Field	Description
Serial Port A	Configures the selected serial port. You can select one of these: • **Auto (default)**: Either the BIOS or OS configures the serial port. • **Disabled**: The serial port (COM A) is not configured. If you select this option, you must also set the Com Port Address option on the Console Redirection sub-menu to "On-board COM A". • **Enabled**: The user configures the serial port. If you select this option, you must also set the Com Port Address option on the Console Redirection sub-menu to "Disabled".

Boot menu

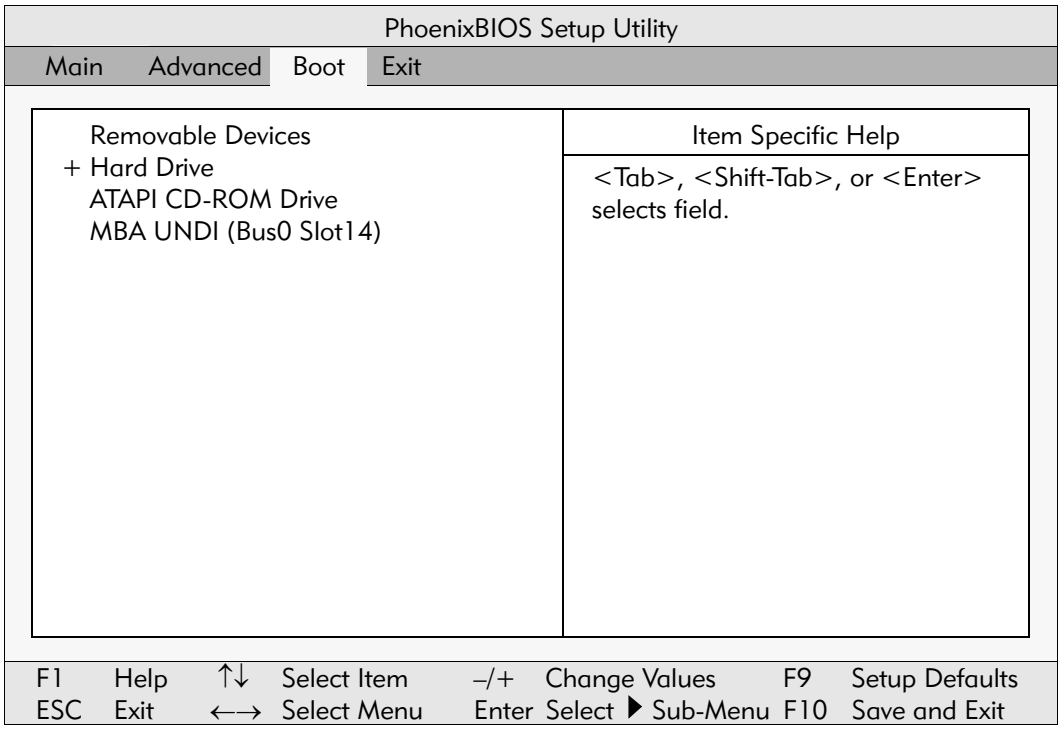
The Boot menu:

- Specifies the order in which the system tries to boot from devices attached to the system.
- Specifies the boot order of devices in the same class, such as hard drives.

Boot order is assigned from top to bottom, with the uppermost enabled boot device in each class being the boot candidate from that device class.

When two devices appear in a class, only the topmost item is available as a boot device.

Figure 4-11. Boot menu



To move an item to a higher level in the list, highlight the item and then press the "+" key. To move an item to a lower level in the list, highlight the item and then press the "–" key.

To display all boot device sub-menus under all respective device types, press the Ctrl and Enter keys at the same time.

To display a sub-menu that lists all devices of a specified type available on the system, highlight the device type and press the Enter key. If more than one device of that type exists, use the "+" and "–" keys to change the boot order within the given device type.

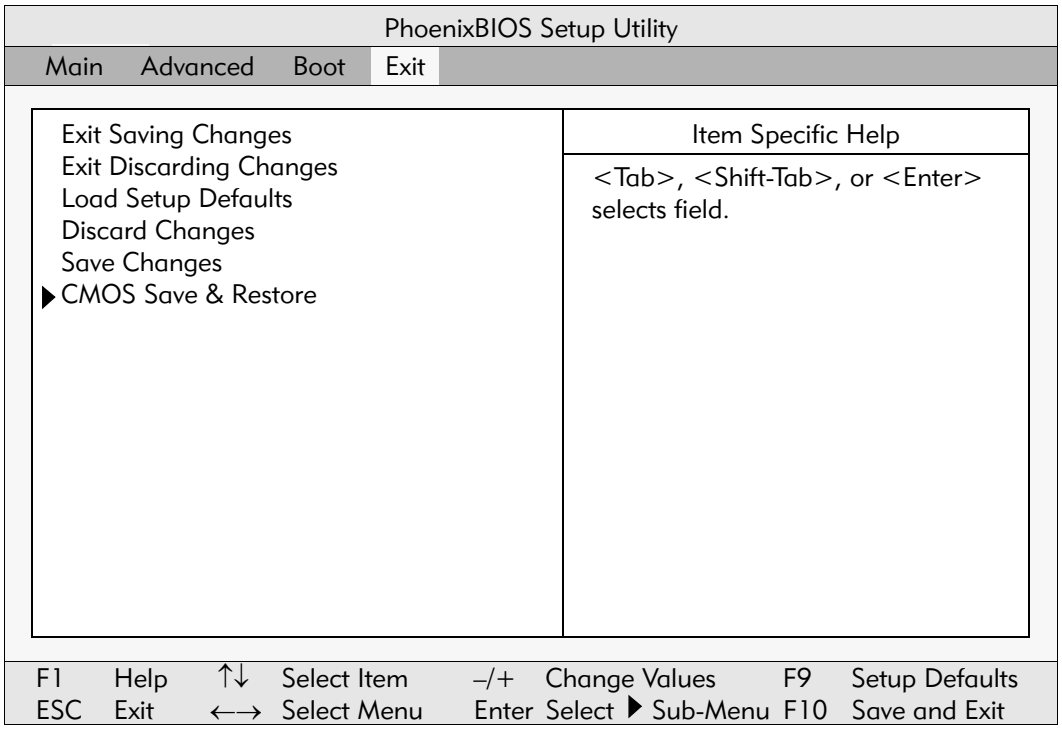
To enable a device, highlight the desired device and press the Shift and 1 keys. An exclamation point (!) displays to the left of enabled devices. To disable a device. highlight the device, then press the Shift and 1 keys again.

Field	Description
Boot order	Determines the boot order of boot devices. This is the default boot order: 1. Removable Devices 2. Hard Drive 3. ATAPI CD-ROM Drive 4. MBA UNDI (Bus 0 Slot 14)

Exit menu

Use the options in this menu to save and exit, or abandon your changes and exit to the system.

Figure 4-12. Exit menu

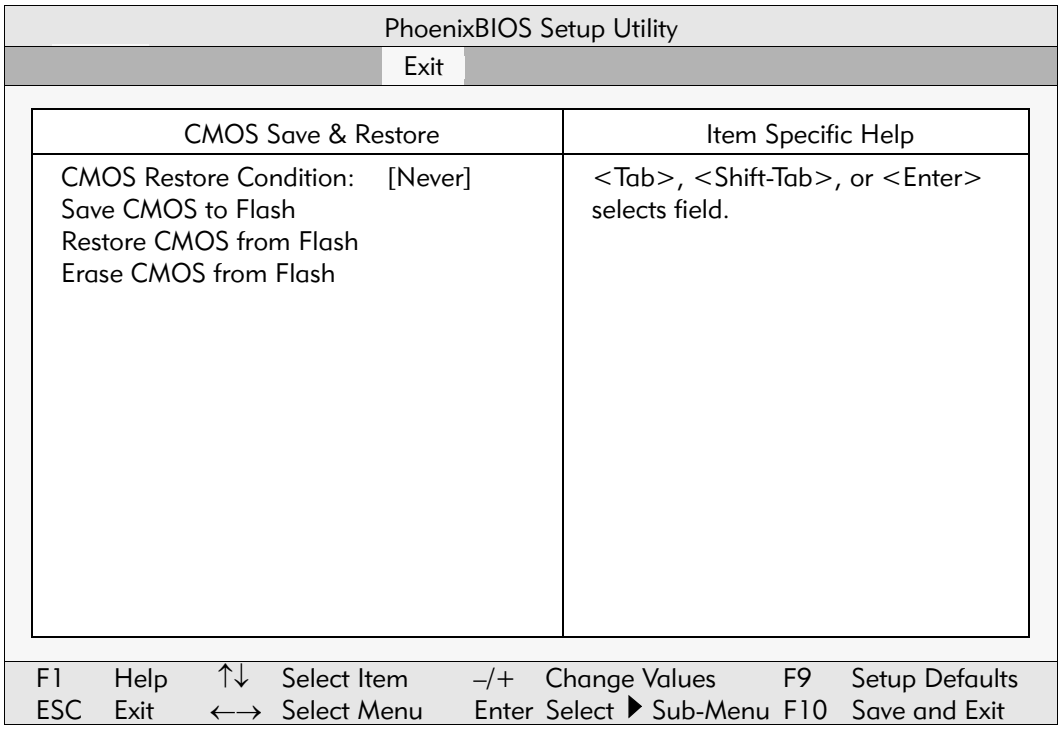


Field	Description
Exit Saving Changes	Saves into CMOS the values you just entered and exits the Setup program. The new values load, and the system reboots.
Exit Discarding Changes	Discards the changes you just made and reverts to the BIOS as it was before you entered the BIOS Setup program. The system boots with the old values.
Load Setup Values	Resets the BIOS values to the original, default values set at the factory, before any suppliers or other end users made changes.
Discard Changes	Loads the system with the values that existed before this editing session started. You do not exit.
Save Changes	Saves to CMOS the edits you made during this session but does not exit the Setup program.
CMOS Save & Restore sub-menu	Displays a menu that controls how the system handles CMOS values. For more information, see *CMOS Save & Restore sub-menu* on page 49.

CMOS Save & Restore sub-menu

Use the options in this menu to save, restore, or erase CMOS settings in the FBD (Flash Boot Device).

Figure 4-13. CMOS Save & Restore sub-menu



Field	Description
CMOS Restore Condition	Determines the conditions under which the BIOS restores CMOS RAM from the FBD when booting. You can select one of these: • CMOS Corruption • Never (default) • Always. Select this option if your system does not have battery backup.
Save CMOS to Flash	Immediately saves current settings in the Setup program to CMOS RAM and into the FBD. This process may take several seconds to complete. **Note**: Always select this option *before* restoring CMOS from Flash.
Restore CMOS from Flash	Immediately restores CMOS RAM and current settings in the Setup program from the FBD. **Note**: This option is available only if the CMOS was previously saved to the FBD.
Erase CMOS from Flash	Immediately erases the CMOS image stored in the FBD.

5 Theory of operation

The EPC-6315 has an Intel Tualatin 512K LP microprocessor with 800 MHz core frequency. The EPC-6315 interfaces through the PCI bus and the system's proprietary interfaces. The RadiSys 82600 chipset provides the memory, PCI, IDE, and serial port interfaces. The Intel 82559 PCI controller provides on-board Ethernet.The EPC-6315 complies with the *Processor PMC standard* VITA 32-199X, Draft 0.41.

Along with any configuration files and other information provided by RadiSys, the EPC-6315 can run DOS 6.22, VxWorks† 5.4, and MontaVista† Linux† Carrier Grade Edition 2.1 operating systems.

- For MV Linux LSPs, contact MontaVista at this URL:
  http://www.mvista.com
- For VxWorks BSPs, contact RadiSys or WindRiver
  http://www.windriver.com
  http://www.radisys.com

The design for the external interface PCI bus is compatible with the PCI Specification, Revision 2.2.

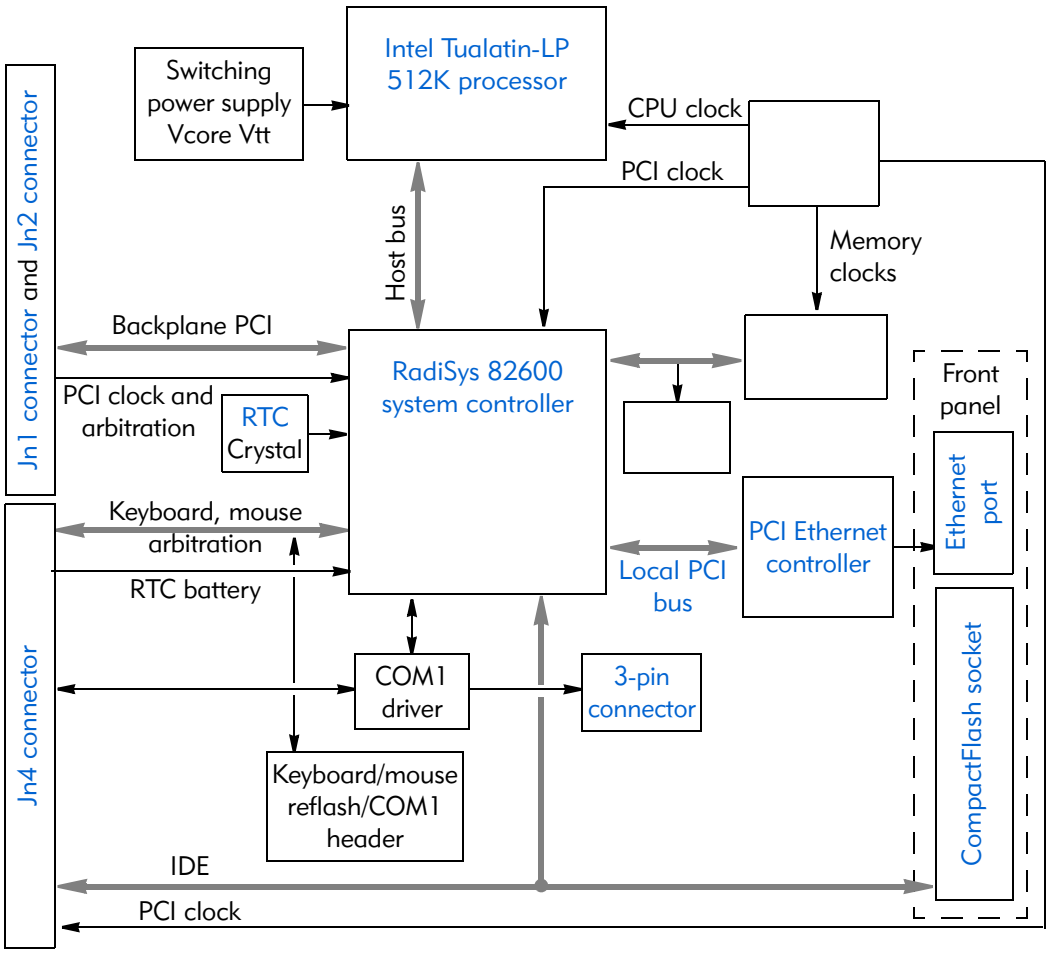
When reading this file online, you can immediately view information about any EPC-6315 topic by placing the mouse cursor over the topic name and clicking:

Organization

Block diagram

The next figure shows the division and interconnection of EPC-6315 functions. The following sections provide detailed descriptions of these items.

Figure 5-1. EPC-6315: block diagram



Intel Tualatin-LP 512K processor

The EPC-6315, designed around the Intel Tualatin 512K LP processor in a micro-FCBGA package, uses Intel's advanced 0.13-micron process technology with copper interconnect.

The Tualatin 512K processor offers high performance and low-power consumption.

The processor's internal speed is 800 MHz, with a 133 MHz system bus frequency at +1.15 V core voltage.

Speed and voltages

The 512 Kbit integrated level 2 (L2) cache based on Advanced Transfer Cache with Error Correcting Code (ECC) architecture runs at the processor core speed and is designed to help improve performance. It complements the system bus by providing critical data faster and by reducing total system power consumption.

The processor's 64-bit wide Assisted Gunning Transceiver Logic (AGTL) system bus provides a glueless, point-to-point interface for the RadiSys 82600 chipset.

The Intel Tualatin 512K LP processor runs at a fixed 800 MHz internal speed with 133 MHz Processor Side Bus (PSB). Speed step is not supported. Optional permanent speed throttling is available.

The EPC-6315 requires two distinct voltages:

- AGTL (VCCT) termination voltage (+1.25V).
- CPU core (VCORE) voltage (+1.15V).

It also requires an AGTL reference voltage (VREF) that should be two thirds the AGTL termination voltage. This is accomplished using a resistor divider.

A high-efficiency switching regulator produces the appropriate processor VCore and Vcct required. Maximum power draw for the EPC-6315 on an 800 MHz Tualatin 512K LP processor is 17.0W.

EPC-6315 power consumption varies with activities the EPC-6315 performs.

Clocking

The EPC-6315 uses an AMI clock generator to generate system clocks. This clock generator has a spread-spectrum feature that is enabled through SMB bus programming.

Clocks	How many	Speed	Purpose
EPC-6315 bus clock[1]	3	133 MHz	Provides timing for the EPC-6315, 82600 chipset, and debug ITP port.
SDRAM clock[1]	8	133 MHz	Supplies on-board memory.
LPCI clock[1]	8	33 MHz	Provides for on-board Ethernet.
Carrier card clock	1	33 MHz	Provides for LPCI.
		66 MHz	Provides for BPCI.
REF clock	2	14.318 MHz	Provides for clock generator and the 82600 chipset.
APIC clock	1	33.33 MHz	Used for 82600 interrupt controller.

[1] The EPC-6315 supports only the 133 PSB and SDRAM clock frequency.

[2] The EPC-6315 contains either a 33 or 66 MHz carrier card clock.

RadiSys 82600 system controller

The 82600 is a highly integrated chipset. In an embedded Intel Architecture I/O system, the 82600 replaces four components: North Bridge, South Bridge, PCI-to-PCI Bridge and Super I/O. The chip includes:

- **Processor/Host bus support**
  Compatible with Intel Pentium processors.
  GTL bus driver technology.
  Support for 66MHz, 100MHz, and 133MHz processor side and memory buses.
- **Integrated SDRAM controller with direct Flash support:**
  Support for 256Mb or 512Mb SDRAM technology.
  16MB to 2GB of main memory.
  7.8, 15.6, and 125 microsecond refresh rates supported.
  ECC support with automatic single bit error "scrub", multiple bit error detect.
  Flash BIOS allowed on SDRAM bus.
- **Dual PCI bus architecture:**
  Independent local and backplane PCI buses with integrated virtual PCI to PCI bridge.
  Provides isolation between local and backplane peripherals.
  Asynchronous operation of both PCI buses.
  Supports concurrent EPC-6315, local PCI and backplane PCI transactions.
- **Local PCI bus:**
  33MHz interface.
  3.3V and 5V, PCI 2.2 compliant.
  5 BREQ/BGNT pairs.
- **Backplane PCI (BPCI) bus:**
  PCI Rev. 2.2, 3.3V and 5V, 33/66MHz interface compliant.
  7 BREQ/BGNT pairs.
  May supply all PCI central resource functions; these functions can be disabled for non-Monarch applications.
- **Integrated core PC logic:**
  Includes all legacy PC/AT compatible peripherals.
  Two 82C59 interrupt controllers.
  Two 82C37 DMA controllers.
  82C54 timer/counter.
  74LS612 address mapper.
- **Real-time clock:**
  256 byte battery backed CMOS SRAM.
- **Integrated peripherals:**
  Ultra DMA/66 EIDE interface.
  COM1 and COM2 support with 16550 compatible UARTs.
  PS/2 compatible keyboard and mouse ports.
  SMBus host interface.
- **Power Management Support.**

- **Integrated Watchdog Timer:**
  Detects system lockup.
  Flexible hardware reset or interrupt on timeout.
- **General Purpose Digital I/O:**
  Multiplexed with other pin functions.
  576 pin BGA package.

The 82600 does not support the LOCK function on the local PCI or the BPCI buses.

Power-up configuration

The following 82600 configuration options are determined during a PWRGOOD reset, using pull-up or pull-down resistors on memory address lines:

Table 5-1. Power-up configuration settings

Address		Description		
ADDR0	10K pull-down	General-purpose I/O pins on the 82600 are used as EIDE data bus. (Default = EIDE).		
ADDR1	10K pull-down	General-purpose I/O pins are used for bus arbitration signals ~BREQ[6:3] and ~BGNT[6:3]. (Default: GPIO).		
ADDR2 and ADDR5		Combination determines Monarch/non-Monarch mode as shown below.		
		ADDR2	**ADDR5**	**Mode**
		0	0	Central resource with arbiter.[1]
		1	0	Peripheral (non-Monarch).
		0	1	Central resource without arbiter (Monarch).
		1	1	Not allowed.
ADDR3	10K pull-down	The Real Time Clock (RTC) is enabled. (Default: Enable).		
ADDR4	10K pull-down	The BIOS is located on the SDRAM bus. (Default: BIOS on SDRAM bus).		
ADDR6	10K pull-down	Multiplexed pins are used for the memory ECC function; the COM2 port is disabled. (Default: ECC).		
ADDR7	10K pull-down	General-purpose I/O pins are used for the serial port, COM1 function. (Default = COM1).		
ADDR8	10K pull-down	The I/O queue depth is set to 8. (Default: 8).		
ADDR10	10K pull-down	SB frequency, only 133 MHz PSB is supported (Default: set to 133MHz).		
ADDR11	10K pull-down	PSB frequency, only 133 MHz FSB is supported.		

[1] This non-standard option is provided by resistor strapping options.

Host bridge

The 82600 connects directly to the AGTL CPU local bus. The processor die includes termination resistors. The 82600 segregates bus transactions as follows:

- 36 address-bit references
- SDRAM references
- LPCI bus cycles
- BPCI bus cycles
- Internal register
- Special cycle (includes halt/shutdown, cache flush, etc.)
- Interrupt acknowledge

Memory subsystem

The memory design for the EPC-6315 has one bank capable of 256 or 512 MB, 133 MHz on the EPC-6315.

The memory bank consists of nine 256Mbit or 512Mbit SDRAM chips, in a x8 organization. The ninth memory chip supports ECC.

The SPD (Serial Presence Detect) PROM provides the memory configuration data. The SPD is an I2C serial PROM that resides on the 82600 SMBus. To determine the computer's memory configuration, BIOS queries the SPD during POST. SPD in the system with 256 MB or 512 MB memory is assigned to address 010 I2C.

Memory map

Physical address space for the system is managed by the 82600 as set up by the System BIOS. That configuration is defined in the following table.

Table 5-2. Memory map

First	Last	Comments
0000 0000h	0009 FFFFh	DOS compatibility region
000A 0000h	000B FFFFh	VGA buffer
000C 0000h	000C BFFFh	VGA BIOS extension (shadowed; if used)
000C C000h	000C FFFFh	Main memory
000D 0000h	000D FFFFh	Main memory
000E 0000h	000F FFFFh	System BIOS (shadowed)
0010 0000h	00EF FFFFh	Main memory
00F0 0000h	00FF FFFFh	Main memory
0100 0000h	0FFF FFFFh[1] 1FFF FFFFh[2]	Main memory
1000 0000h[1] 2000 0000h[2]	FFEF FFFFh	Directed to PCI
FFF0 0000h	FFFF FFFFh	System ROM

[1] Applies to systems with 256M memory (the EPC6315-800-256).

2 Applies to systems with 512M memory (the EPC6315-800-512).

BIOS flash support

The re-programmable, 4Mbyte FBD (Flash BIOS Device) consists of 32 128KB blocks. The top 1 Mbyte holds the BIOS while the remainder is available for OEM non-volatile storage.

For a map of the flash chip, see *Appendix E, Flash memory addresses*. For information about re-programming the flash chip, see *Appendix F, Re-programming the flash chip*.

The BIOS Setup program can save and restore a CMOS configuration using storage in the FBD. This feature is useful because the EPC-6315 does not have battery on board. A battery could be installed on the carrier card and connected to the EPC-6315 via pin 62 of the optional JN4 connector. The BIOS CSR function automatically saves and restores CMOS RAM contents to flash since there is no on-board battery on the EPC-6315.

For more information about the BIOS setup program, see *Chapter 4, BIOS configuration*.

Dual PCI bus architecture

The 82600 integrates dual PCI busses, a local and backplane PCI bus. The LPCI (local PCI) bus can operate asynchronously at up-to the host processor's clock rate or down-to one quater of this clock rate. Architecturally, it can be viewed as the high speed private peripheral bus for the processor.

As such, an LPCI bus master cannot access the backplane PCI (BPCI) bus or vice-versa. Whereas the LPCI bus interface always acts as the LPCI central resource bridge, the BPCI interface connects to a "backplane" bus such as a carrier card, and supports Monarch and non-Monarch modes.

The EPC-6315 connects BPCI to a carrier card via the standard Jn1 and Jn2 PMC connectors and is compatible with *Processor PMC Standard*, Vita 32-199X, Draft 8 September 2000, and supports these modes accordingly:

- **Monarch mode:** In this mode it is a main PCI bus processor module, performing PCI bus enumeration after power- up, and interrupt handling. To comply with the PrPMC specification, neither clock generator nor an arbiter reside on the module.

  A resistor strapping option exists to provide a clock from the EPC-6315 to the carrier card through the optional Jn4 connector. This allows a carrier to implement a simple clock buffer to distribute the clocks to other PCI devices on the carrier card. Also, arbitration may be enabled from the 82600 via register strapping options.

- **Non-Monarch mode:** In this mode it is not a main CPU, does not perform PCI bus enumeration, and may generate interrupts to the main CPU. When in this mode, it is possible to configure the EPC-6315 to present some or all of its local memory to the BPCI bus.

  The System BIOS BIOS Setup program provides:

  - Access to memory remapping registers within the 82600. These Setup tokens are visible in both Monarch and non-Monarch modes, but are ignored by the BIOS in Monarch mode. In the Setup program, you can use either the default BIOS settings or any of several custom options.
  - Control of memory windows within the 82600. These Setup tokens are visible in both Monarch and non-Monarch modes, but are ignored by the BIOS in non-Monarch mode. You can choose to use either the System BIOS settings or any of several custom settings.

The Monarch signal (pin 64 of Jn2) defines a Processor PMC as a being Monarch or non-Monarch. The optional EREADY signal is an output of the non-Monarch Processor PMC, indicating that it has completed on-board enumeration and can respond to PCI bus enumeration by the Monarch via configuration cycles.

PCI bus device enumeration depends on the EPC-6315's mode:

- **Monarch:** The System BIOS enumerates the local PCI bus and beyond.

- **Non-Monarch**: The System BIOS configures only the local PCI bus. Setup allows custom programming of the system resources by providing access to two memory windows and two memory remap windows within the RadiSys 82600.

Local PCI bus

The EPC-6315 implements a +3.3V, 32 bit local PCI bus. The bus runs at 33 MHz and has the RadiSys 82600 chipset as the central resource. This PCI bus has one peripheral device connected to it, the Intel 82559 Ethernet controller.

The next table describes on-board device PCI configuration space locations. The IDSEL pin on each device connects to the listed PCI address pin. To select the configuration registers of a given device, a PCI Configuration Space access must be made with the device's corresponding IDSEL address bit set.

Table 5-3. PCI device configuration

Peripheral	~IDSEL	Device	Function	INT	LPCI arbitration ~REQ/~GNT
RadiSys 82600 system controller/local PCI bridge	AD11	0	0	–	Internal
EIDE		0	1	D	Internal
Backplane PCI bridge (master only)	AD12	1	0		Internal
Intel 82559 Ethernet A controller	AD25	14	0	A	0

PCI Ethernet controller

One Intel 82559 fast Ethernet controller incorporates internal Media Access Controller (MAC) and Physical Interface (PHY) interfaces providing support for 10BASE-T or 100BASE-TX connections to the front panel RJ45 connector. The controller uses local PCI interrupt A, ~REQ0/~GNT0 arbitration pairs, and has a standard PCI 2.1 compliant configuration space allowing system identification and configuration.

The PHY enables direct connection to the network media using a 25 MHz, 25 ppm crystal to derive its internal transmit digital clocks. An Intel- defined magnetics interfaces the PHY with the RJ45 connection (located on the front panel). In 100BASE-TX mode, the analog subsection of the PHY performs these functions:

- Converts received analog data from the RD pair into a digital 125 Mbps stream, recovering both clock and data.
- Converts a digital 125 Mbps stream into the proper format, and drives it through the TD pair into the physical medium.

The 82559 drives on-board status LEDs directly.

PCI interrupts

The EPC-6315 has two sets of PIRQ[A:D] interrupts, one set for the local bus (LPIRQ) and one for the backplane PCI bus (BPIRQ).

IDE controller flash disk

One device on the primary EIDE channel is a single CompactFlash connector without an ejector. The CompactFlash module acts similar to an IDE drive, and provides additional mass storage.

An additional EIDE interface is provided via the optional Jn4 connector to IDE device on test or baseboard.

Bus termination resistors are required on the carrier card adjacent to Jn4 to avoid unwanted transmission line affects of the IDE cable set. For detailed information, see *Appendix G, Carrier card design*.

RTC

The RadiSys 82600 provides an internal Real Time Clock (RTC) and 256 byte CMOS RAM functions. These perform the following functions:

- Tracks time of day.
- Stores system data during a system power-down.

The RTC operates on a 32.768 KHz crystal with better than or equal to 50ppm stability.

As part of the 82600, the RTC is limited to +2.5V. A battery connection is provided via “battery pwr” (pin 60) on the Jn4 connector; no battery is provided on the EPC-6315. The RTC and CMOS RAM are addressable at the standard PC/AT architecture I/O addresses, 70h and 71h. Interrupts are signaled on IRQ8. For more information, see *CMOS Save & Restore sub-menu* on page 49.

Serial port

The 82600 includes two 16C550 UARTs. You can enable one as COM1, and the other as COM2. You can configure the COM1 port to support IRDA at data rates up to 115Kbaud. As in a standard PC, COM1 is accessed in the I/O address space at 0x3f8-3ff and signals interrupts on IRQ4. The configurable port shares eight pins with the SDRAM ECC pins. The COM2 port pins are not available externally and COM2 must be disabled (Default for the EPC-6315).

SERIRQ protocol is not supported, as it only responds to the devices on the LPCI bus.

Keyboard and mouse controller

The 82600 contains a PC/AT compatible keyboard controller with PS/2 compatible mouse controller extensions. If not needed, or if an external keyboard controller is desired, it may be disabled.

The keyboard controller clock is generated from HCLK. Response to keyboard commands is immediate—usually within one keyboard clock—because this function is implemented internally as a hard-wired state machine.

Power

The next table represents the estimated EPC-6315 power consumption.

This table includes the power requirements for the dual-die, +3.3V, nine SDRAM ICs.

Table 5-4. Power estimates

		Watts	
Product configuration	**Voltage**	**Maximum**	**Typical[1]**
EPC6315-800-512	+3.3V	6.0W	4.8W
(800Mhz CPU, 133Mhz PSB, 512MB)	+5V	11.0W	8.8W
Total power		**17.0W**	**13.6W**
EPC6315-800-256	+3.3V	4.5W	3.6W
(800Mhz CPU, 133Mhz PSB, 256MB)	+5V	11.0W	8.8W
Total power		**15.5W**	**12.4W**

[1] Typical power measurement is 80% of maximum.

The 82600's core logic of +2.5V is supplied by a linear regulator working from +5V. The expected load current is 400mA.

The RTC portion of the 82600 is also limited to +2.5V. The RTC power pin is therefore supplied through:

- A silicon diode connected to the +3.3V supply, and
- A silicon diode connected to a +3.0V Lithium button cell via optional Jn4 connector to the baseboard.

Power to EPC-6315 VCORE +1.15 V and VCCT +1.25V is supplied by a Linear Technologies LTC1703 dual synchronous switching regulator along with external FETs. The LTC1703 5 VID inputs are fixed with resistors to produce an output voltage (VCORE) of +1.15V on the first controller. The second controller sets up its output voltage through a resistor divider network to +1.25V, the AGTL termination voltage, VCCT. LTC1703 can provide up to 25A output current per channel. The current limit is set to 15 A for VCORE, and to 5 A for VCCT. The expected maximum load current is 7A for VCORE.

A precision voltage reference in conjunction with a voltage comparator provides monitoring of the +5V and +3.3V supplies. The outputs of the comparators connect directly to the soft-start inputs for the switching regulator that creates VCORE and VCCT. As soon as +3.3V and +5V planes are fully charged, the switcher begins to power on and VCCT, and after VCCT is stable, VCORE comes up. Voltage comparators monitor the status of VCORE, VCCT, +2.5V, +1.8V, and +1.5V power. The outputs of the comparators are tied to the system power good line and cause system reset on power failure. As soon as the voltages are valid, the board comes out of reset.

Avoiding memory address and data misalignment

All the conditions described in the situation below must occur at the correct time for this to be experienced. The situation is possible, but unlikely to occur.

Under the following precise heavy host and PCI bus loading conditions, memory from either the LPCI or BPCI interface can be corrupted:

1. **PCI peripheral writes:** Many “small writes” from a PCI peripheral or multiple PCI peripherals that target the 82600 memory. The 82600 has two seperate FIFOs for both LPCI and BPCI to host bus transactions: an address FIFO (four entires) and a data FIFO (64 bytes). If PCI peripherals perform large writes (e.g. 32 bytes or more with each transaction) targeted at the 82600, then the 82600 data FIFO fills up and throttles further PCI target transactions (this avoids the address FIFO problem).
2. **Host bus traffic:** Large amounts of host bus traffic that keeps 82600 from servicing the PCI to host address and data FIFOs (so that the address FIFO can “stack up”).
3. **PIII host read requests:** The PIII host makes a read request (that is deferred) to the PCI bus through the 82600 at just the “right” (or wrong, depending upon your point of view) instant.
4. **Unaligned PCI peripheral writes:** PCI peripheral initiated "small writes" must be unaligned and/or span an 8-byte boundary, but yet not be a naturally aligned 16 byte or 32 byte chunk (needs to require at least 2 host addresses to complete the single PCI write in the host domain - for example a 24 byte write that starts at address 0x80 would require two host bus writes: a 16 byte starting at 0x80 and an 8 byte starting at 0x90 ... the host bus doesn't support 24 byte writes).
5. **I/O queue depth:** I/O queue depth must be set to 1 or 8.
6. **L2:** Disabling L2 makes it more difficult to expose the timing problem.

If at least 1 through 4 occur, then a “write access” address targeting the 82600 from the PCI bus may not be “saved” in the address FIFO, but data associated with the write is saved in the data FIFO. Later, when the address and data FIFOs are “popped,”,a “newer” PCI address appears with the older data on the host bus (the PCI address that went with the older data didn’t get saved). And all subsequent PCI write access addresses will be similarly misaligned with the data.

As a workaround, you can set host bus I/O queue depth to 1 (instead of 8). This approach requires the addition of 1 each pull-up resistor on memory address 8.

For detailed information, see these RadiSys 82600 documents, available on the RadiSys web site:

- *82600 High Integration Dual PCI System Controller Data Book*
- *82600 High Integration Dual PCI System Controller Errata*

A Message codes

This appendix lists the Phoenix BIOS 4.06 standard POST error codes which can generate console messages.

Class	Number	Name
Disk errors	200h	ERR_DISK_FAILED
Keyboard errors	210h	ERR_KBD_STUCK
	211h	ERR_KBD_FAILED
	212h	ERR_KBD_KCFAIL
	213h	ERR_KBD_LOCKED
Video errors	220h	ERR_VIDEO_SWITCH
Memory errors	230h	ERR_SYS_MEM_FAIL
	231h	ERR_SHAD_MEM_FAIL
	232h	ERR_EXT_MEM_FAIL
	233h	ERR_MEM_TYPE_MIX
	234h	ERR_MEM_ECC_SINGLE
	235h	ERR_MEM_ECC_MULTIPLE
	236h	ERR_MEM_DECREASED
	237h	ERR_DMI_MEM_FAIL
POS/timeout errors	240h	ERR_POS
CMOS errors	250h	ERR_CMOS_BATTERY
	251h	ERR_CMOS_CHECKSUM
Timer errors	260h	ERR_TIMER_FAILED
Real-time clock errors are x70h	270h	ERR_RTC_FAILED
Invalid date time	271h	ERR_RTC_INV_DATE_TIME
Configuration errors	280h	ERR_CONFIG_FAILED
	281h	ERR_CONFIG_MEMORY
NVRAM errors	290h	ERR_NVRAM
Diskette errors	2B0h	ERR_FLOPPYA_FAILED
	2B1h	ERR_FLOPPYB_FAILED
	2B2h	ERR_FLOPPYA_INCORRECT
	2B3h	ERR_FLOPPYB_INCORRECT
Load errors	2C0h	ERR_LOADED
Cache errors	2D0h	ERR_CACHE_FAILED

Class	Number	Name
System memory exceeds CPU caching limit	2D1h	ERR_L2_CACHE_RANGE
IO errors	2E0h	ERR_IO_ADDRESS
	2E1h	ERR_IO_COM
	2E2h	ERR_IO_LPT
	2E3h	ERR_IO_CONFLICT
	2E4h	ERR_IO_UNSUPPORTED
	2E5h	ERR_IO_IRQ
	2E6h	ERR_IO_IDE
	2E7h	ERR_IO_FDD
	2F0h	ERR_OTHER_CPUID
	2F1h	ERR_OTHER_BIST
	2F2h	ERR_OTHER_BSP
	2F3h	ERR_OTHER_AP
	2F4h	RR_OTHER_CMOS
	2F5h	ERR_OTHER_DMA
	2F6h	ERR_OTHER_NMI
	2F7h	ERR_OTHER_FAILSAFE

B Interrupts

The next table shows EPC-6315 interrupt assignments. This routing is implemented by the RadiSys 82600 embedded chipset.

Table B-1. Interrupts

Interrupt	Description
IRQ0[1]	System timer (internal connection)
IRQ1[1]	Keyboard controller (internal connection)
IRQ2	Cascade interrupt input (internal connection)
IRQ3[2]	
IRQ4[1, 2]	COM1 (internal connection)
IRQ5[2]	
IRQ6	
IRQ7	
IRQ8[1]	Real-time clock (internal connection)
IRQ9[1, 2]	SMBus, reset switches, power management, DMA, BIST (via Serial IRQ)
IRQ10[2]	Soft reset is imminent via serial IRQ from Watchdog
IRQ11[2]	
IRQ12[1, 2]	PS/2 mouse (internal connection)
IRQ13	Numeric coprocessor ~FERR (internal connection)
IRQ14[1]	Primary IDE channel
IRQ15[2]	
NMI[1]	When ~SERR or ~IOCHK is asserted (software controlled)
SMI	Power management or ECC error
PIRQA	
PIRQB	
PIRQC	
PIRQD[1]	PCI ~INTD

[1] You cannot move these items.

[2] You can include these items in the PCI interrupt pool.

Note that PIRQ[A–D] correspond directly to the PCI interrupts INT[A–D]. The software may steer these interrupts to any of the 11 interrupts (IRQ[15, 14, 12–9, 7–3]) using the Interrupt Route Control register.

For detailed information, see *Chapter 4, BIOS configuration*.

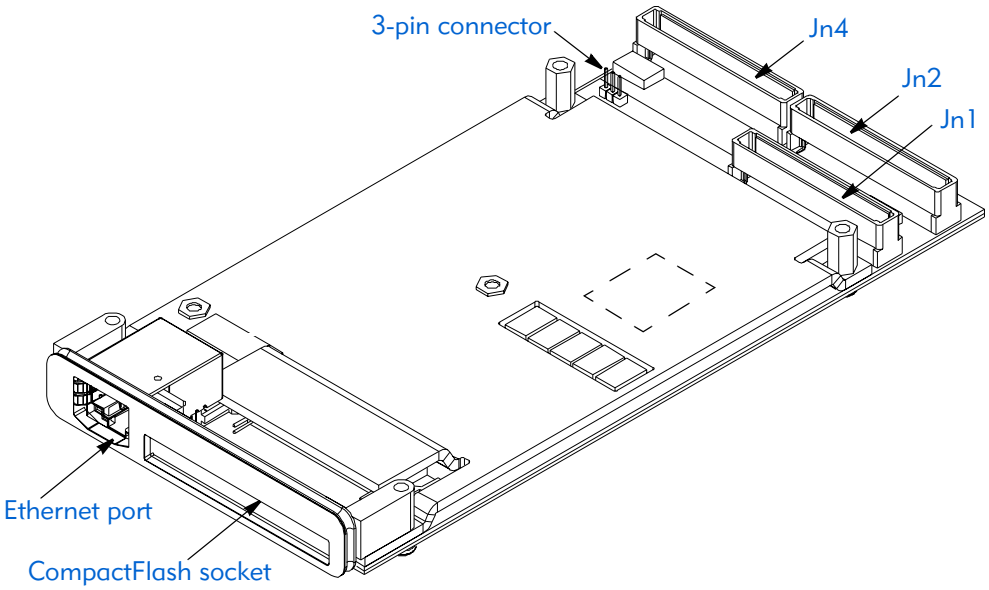
C Connectors

This appendix details the connectors used by the EPC-6315 and gives the signal pinout of each connector.

Connector locations

The next figure shows the locations of connectors on the EPC-6315:

Figure C-1. EPC-6315: connectors



Signals used for a purpose other than that identified in the appropriate specification are noted as follows:

XYZ / NC

Specified use — RadiSys use

CompactPCI connector

J1 connector

The CompactPCI J1 connector is a female 2mm-pitch 6 column by 25 row right angle Hard Metric (HM) connector with a guide lug in the center.

Table C-1. CompactPCI J1 connector pin definitions

Pin	A	B	C	D	E	F[8]
1	**+5V**	**–12V**	NC (~TRST)[13]	**+12V**	**+5V**	**GND**
2	NC (TCK)[13]	**+5V**	NC (TMS)[14]	NC (TDO)[14]	NC (TDI)[14]	**GND**
3	~INTA	~INTB	~INTC	**+5V**	~INTD	**GND**
4	IMPI SMB PWR IN	Healthy	V(I/O)	INTP	INTS	**GND**
5	BRSV[11]	BRSV[11]	~RST	**GND**	~GNT	**GND**
6	~REQ	**GND**	**+3.3V**	CLK	AD[31]	**GND**
7	AD[30]	AD[29]	AD[28]	**GND**	AD[27]	**GND**
8	AD[26]	**GND**	V(I/O)	AD[25]	AD[24]	**GND**
9	~C/BE[3]	IDSEL	AD[23]	**GND**	AD[22]	**GND**
10	AD[21]	**GND**	**+3.3V**	AD[20]	AD[19]	**GND**
11	AD[18]	AD[17]	AD[16]	**GND**	C/~BE[2]	**GND**
12–14			Key area			
15	**+3.3V**	~FRAME	~IRDY	~BD_SEL[7]	~TRDY	**GND**
16	~DEVSEL	**GND**	V(I/O)[(2)(6)]	~STOP	~LOCK	**GND**
17	**+3.3V**	IPMB_CLK	IPMB_DAT	**GND**	~PERR	**GND**
18	~SERR	**GND**	**+3.3V**	PAR	C/~BE[1]	**GND**
19	**+3.3V**	AD[15]	AD[14]	**GND**	AD[13]	**GND**
20	AD[12]	**GND**	V(I/O)[(2)]	AD[11]	AD[10]	**GND**
21	**+3.3V**	AD[9]	AD[8]	M66EN[5]	C/~BE[0]	**GND**
22	AD[7]	**GND**	**+3.3V**	AD[6]	AD[5]	**GND**
23	**+3.3V**	AD[4]	AD[3]	**+5V**	AD[2]	**GND**
24	AD[1]	**+5V**	V(I/O)[2]	AD[0]	~ACK64	**GND**
25	**+5V**	~REQ64	~ENUM	**+3.3V**	**+5V**	**GND**

PMC connectors

The main board supports a backplane via standard Jn1 and Jn2 PMC connectors. The PMC site provides power for +3.3V, +5V, +12V and –12V. The PCI interface uses +3.3V signaling, but is +5V tolerant. This allows VIO to connect to +5V or +3.3V on the EPC-6315.56. ±12V is not used on the board. However, AC bypass is provided to these pins.

Jn1 connector

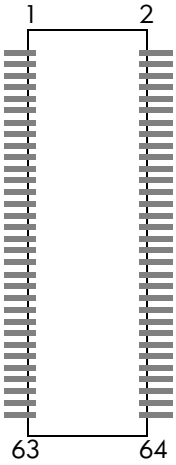


Table C-2. Jn1 connector pin definitions

Pin	Signal	Signal	Pin
1	TCK	**–12V**	2
3	**GND**	~INTA	4
5	~INTB	~INTC	6
7	~Busmode1	**+5V**	8
9	~INTD	PCI-Reserved	10
11	**GND**	**+3.3V**	12
13	PCICLK	**GND**	14
15	**GND**	~GNT0	16
17	~REQ0	**+5V**	18
19	V(I/O)	AD[31]	20
21	AD[28]	AD[27]	22
23	AD[25]	**GND**	24
25	**GND**	~C/BE[3]	26
27	AD[22]	AD[21]	28
29	AD[19]	**+5V**	30
31	V(I/O)	AD[17]	32
33	~FRAME	**GND**	34
35	**GND**	~IRDY	36
37	~DEVSEL	**+5V**	38
39	**GND**	~LOCK/NC	40
41	~Sdone/NC	~SBO/NC	42
43	PAR	**GND**	44
45	V(I/O)	AD[15]	46
47	AD[12]	AD[11]	48
49	AD[09]	**+5V**	50
51	**GND**	~C/BE[0]	52
53	AD[06]	AD[05]	54
55	AD[04]	**GND**	56
57	V(I/O)	AD[03]	58
59	AD[02]	AD[01]	60
61	AD[00]	**+5V**	62
63	**GND**	~REQ64/NC	64

Jn2 connector

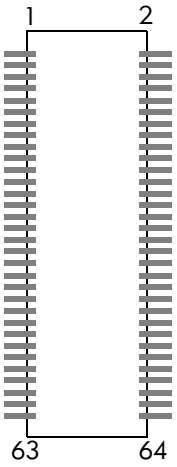


Table C-3. Jn2 connector pin definitions

Pin	Signal	Signal	Pin
1	**+12V**	~TRST	2
3	TMS	TDO	4
5	TDI	**GND**	6
7	**GND**	PCI-Reserved	8
9	~SERIRQ/NC	PCI-Reserved	10
11	~Busmode2	**+3.3V**	12
13	~RST	~Busmode3/NC	14
15	**+3.3V**	~Busmode4/NC	16
17	~PME	**GND**	18
19	AD[30]	AD[29]	20
21	**GND**	AD[26]	22
23	AD[24]	**+3.3V**	24
25	IDSEL	AD[23]	26
27	**+3.3V**	AD[20]	28
29	AD[18]	**GND**	30
31	AD[16]	C/~BE[2]	32
33	**GND**	IDSELB/NC	34
35	~TRDY	**+3.3V**	36
37	**GND**	~STOP	38
39	~PERR	**GND**	40
41	**+3.3V**	~SERR/NC	42
43	C/~BE[1]	**GND**	44
45	AD[14]	AD[13]	46
47	M66EN	AD[10]	48
49	AD[08]	**+3.3V**	50
51	AD[07]	~GNT2/NC	52
53	**+3.3V**	~REQ2/NC	54
55	PMC-Reserved	**GND**	56
57	PMC-Reserved	~ENUM/NC	58
59	**GND**	RSTOUT/NC	60
61	~ACK64	**+3.3V**	62
63	**GND**	PMC-Reserved	64

Jn4 connector

The PMC user-defined optional connector, Jn4, routes a set of standard peripheral signals such as EIDE, COM, keyboard, and mouse as well as PCI signals for four ~REQ/~GNT pairs and one BPCI clock.

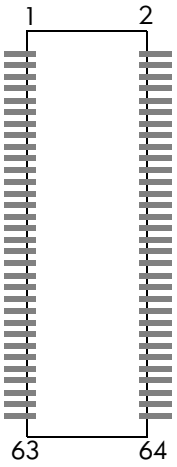


Table C-4. Optional JN4 connector pin definitions

Pin	Signal	Signal	Pin
1	~RST	D8	2
3	D7	D9	4
5	D6	D10	6
7	D5	D11	8
9	D4	D12	10
11	D3	D13	12
13	D2	D14	14
15	D1	D15	16
17	D0	**GND**	18
19	**GND**	CS0	20
21	~IOW	CS1	22
23	~IOR	A0	24
25	IORDY	A1	26
27	~IRQ14	A2	28
29	**GND**	**GND**	30
31	USBP1–	USBP0–	32
33	USBP1+	USBP0+	34
35	**GND**	**GND**	36
37	KCLK	KDATA	38
39	COM,~DTR	COM,~DSR	40
41	COM, ~DCD	COM,~RxD	42
43	COM,~TxD	COM,~CTS	44
45	COM,~RTS	COM,~RI	46
47	**+5V**	MDATA	48
49	~GNT3	~REQ3	50
51	~GNT4	~REQ4	52
53	~GNT5	~REQ5	54
55	~GNT6	~REQ6	56
57	~DASP	~PDIAG	58
59	BPCIREF	**+3.3V**	60
61	MCLK	PWR_BAT_IN	62
63	DMREQ	~DMACK	64

Table C-5. PMC connector Jn4 signal summary

Signal name	Type	Description
A[2:0]	O	**Primary disk address[2:0]**. These signals indicate which byte in either the ATA command block or control block is being addressed. If the IDE signals are configured for Primary and Secondary, these signals are connected to the corresponding signals on the Primary IDE connector. If the IDE signals are configured for Primary 0 and Primary 1, these signals are used for the Primary 0 connector. **During reset**: High-Z **After reset**: Undefined**During POS**: PDA
PCIREF	O	**PCI reference clock**. A clock running at 33 or 66 MHz which provides timing for AT transactions on the PCI bust of Jn1 and Jn2.
COM	I/O	**COM port signals**.
~CS0	O	P**rimary disk chip select for 1F0H–1F7H range**. For ATA command register block. If the IDE signals are configured for Primary and Secondary, this output signal is connected to the corresponding signal on the Primary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, this signal is used for the Primary Master connector. **During reset**: High **After reset**: High **During POS**: High
~CS1	O	**Primary disk chip select for 3F0–3F7 range**. For ATA control register block. If the IDE signals are configured for Primary and Secondary, this output signal is connected to the corresponding signal on the Primary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, this signal is used for the Primary Master connector. **During reset**: High **After reset**: High **During POS**: High
D[15:0]	I/O	**Primary disk data[15:0]**. These dignals transfer data to or from the IDE device. If the IDE signals are configured for Primary and Secondary, these signals are connected to the corresponding signals on the Primary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, this signal is used for the Primary Master connector. **During reset**: High-Z **After reset**: Undefined**During POS**: PDD
DASP	O	**Drive active/slave present**. Indicates CompactFlash activity.

Table C-5. PMC connector Jn4 signal summary

Signal name	Type	Description
~DMACK	O	**Primary disk DMA request**. This input signal is directly driven from the IDE device DMARQ signal. It is asserted by the IDE device to request a data transfer, and used in conjunction with the PCI bus master IDE function. It is not associated with any AT compatible DMA channel. If the IDE signals are configured for Primary and Secondary, this signal is connected to the corresponding signal on the Primary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, this signal is used for the Primary Master connector.
~DMREQ	I	**Primary disk DMA request**. This input signal is directly driven from the IDE device DMARQ signal. It is asserted by the IDE device to request a data transfer, and used in conjunction with the PCI bus master IDE function. It is not associated with any AT compatible DMA channel. If the IDE signals are configured for Primary and Secondary, this signal is connected to the corresponding signal on the Primary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, this signal is used for the Primary master connector.
~GNT[6:3]	O	**PCI bus grant**. Active los assertion indicates that the PCI bus is granted to a particular device.
~IOR	O	**Primary disk to read**. In normal IDE, this is the command to the IDE device that is may drive data onto the PDD[15:0] lines. Data is latched by PIIX4 on the negation edge of ~PDIOR. The IDE device is selected wither by the ATA register file chip selects (~PDCS1, ~PCDS3) and the PDA[2:0] lines, or the IDE DMA sslave arbitration signals (~PDDACK). In an Ultra DMA/33 read cycle, this signal is used as ~DMARDY which is negated by the PIIX4 to pause Ultra DMA/33 transfers. In an Ultra DMA/33 write cycle, this signal is used as the STROBE signal, with the drive latching data on rising and falling edges of STROBE. If the IDE signals are configured for Primary and Secondary, this signal is connected to the corresponding signal on the Primary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, this signal is used for the Primary Master connector. **During reset**: High **After reset**: High **During POS**: High

Table C-5. PMC connector Jn4 signal summary

Signal name	Type	Description
IOW	O	**Primary disk IO write**. In normal IDE mode, this is the command to the IDE device that it may latch data from the PDD[15:0] lines. Data is latched by the IDE device on the negation edge of ~PDIOW. The IDE device is selected either by the ATA register file chip selects (~PDCS1, ~PDCS3) and the PDA[2:0] lines, or the IDE DMA slave arbitration signals (~PDDACK). For Ultra DMA/33 mode, this signal is used as the STOP signal, which terminates an Ultra DMA/33 transaction. If the IDE signals are configured for Primary and Secondary, this signal connects to the corresponding signal on the Primary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, this signal is used for the Primary Master connector. **During reset**: High **After reset**: High **During POS**: High-Z
IORDY	I	**Primary IO channel ready**. In normal IDE mode, this input signal is directly driven by the corresponding IDE device's IORDY signal. In an Ultra DMA/33 read cycle, this signal is used as STROBE, with the PIIX4 latching data on rising and falling edges of STROBE. In an Ultra DMA/33 write cycle, this signal is used as the ~DMARDY signal which is negated by the drive to pause Ultra DMA/33 transfers. If IDE signals are configured for Primary and Secondary, this signal connects to the Primary IDE connector's corresponding signal. If the IDE signals are configured for Primary Master and Primary Slave, thie signal is used for the Primary Master connector. This is a Schmitt triggered input.
~IRQ14	I	**IDE interrupt**. Provides a mechanism for IDE devices to interrupt the processor.
KCLK KDATA		**Keyboard clock and data**.
MCLK MDATA		**Mouse clock and data**.
~PDIAG	I	**IDE slave diagnostic**. Indicates that the IDE slave drive diagnostic is complete.
PWR_BAT_IN	I	**RTC power**. Battery power for real-time clock and CMOS during power down.
~REQ[6:3]	I	**PCI bus request**. Active low assertion indicates a request to become the PCI bus master.
~RST	O	**IDE reset**. Active low assertion indictaes the IDE bus should reset.
USBP0+, USBP0–	I/O	**Serial bus port 0**. This signal pair comprises the differential data signal for USB port 0. **During reset**: High-Z **After reset**: High-Z **During POS**: High-Z
USBP1+, USBP1–	I/O	**Serial bus port 1**. This signal pair comprises the differential data signal for USB port 1. **During reset**: High-Z **After reset**: High-Z **During POS**: High-Z

Ethernet port

The front panel RJ45 connector provides support for 10/100Base-TX Ethernet channel. The RJ45 connector does not contain magnetics and LEDs.

Table C-6. Ethernet pin definitions

Pin	Description	Pin	Description
1	Transmit +	6	Receive –
2	Transmit –	7	**TERM**
3	Receive +	8	**TERM**
4	**TERM**	9	**Shield**
5	**TERM**	10	**Shield**

CompactFlash socket

The 50 pin low profile header provides for Compact Flash card type I.

Table C-7. Compact Flash socket pin definitions

Pin	Signal	Pin	Signal
26	~CD1/**GND**	1	**GND**
27	D11	2	D03
28	D12	3	D04
29	D13	4	D05
30	D14	5	D06
31	D15	6	D07
32	~CE2	7	~CE1
33	~VS1/NC	8	A10/**GND**
34	~IORD	9	~OE/**GND**
35	~IOWR	10	A09/**GND**
36	~WE/**+3.3V**	11	A08/**GND**
37	RDY_BSY/IRQ	12	A07/**GND**
38	**+3.3V**	13	**+3.3V**
39	~MASTER	14	A06/**GND**
40	~VS2/NC	15	A05/**GND**
41	~RESET	16	A04/**GND**
42	~WAIT/IORDY	17	A03/**GND**
43	~INPACK/NC	18	A02
44	~REG/**+3.3V**	19	A01
45	BVD2/~DASP	20	A00
46	BVD1/~PDIAG	21	D00
47	D08	22	D01
48	D09	23	D02
49	D10	24	WP/NC
50	**GND**	25	~CD2/**GND**

3-pin connector

This 3-pin header, when connected via cable to an input device, provides access to the system BIOS.

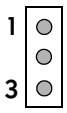


Table C-8. 3-pin connector pin definitions

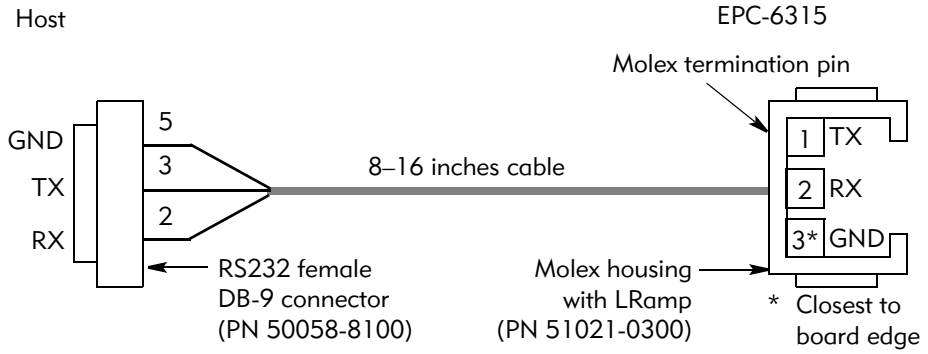
Pin	Signal
1	COM1:TXD
2	COM1:RXD
3	**GND**

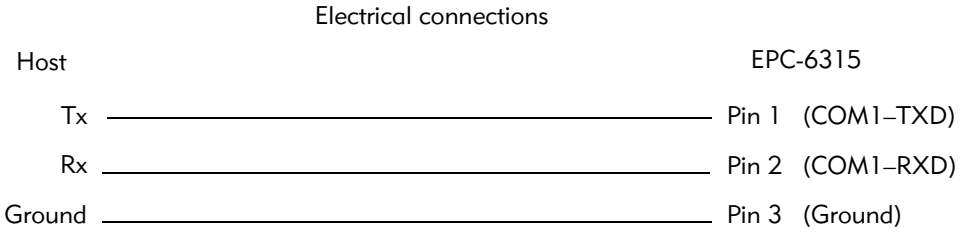
For information about using this connector, see *Using the 3-pin connector* on page 9.

Null-modem serial cable

RadiSys does not supply the serial cable. To assemble the cable, you will need the following:

Item	Part number
3-pin connector	Molex receptacle 51021-0300
Female crimp terminal	Molex 50058-8100
RS232 connector	Standard RS323 female DB-9 serial connector
Recommended cable	Belden 8643 (Round, 3 Conductor, 30 Gage) or Molex Series 6800 (Flat, 3 Conductor, 28 Gage), cut to desired length (i.e. 8- 16 inches)





D Error messages

Upon encountering the following error conditions, the System BIOS tries to display a message on the VGA, and the console when redirected, then halts:

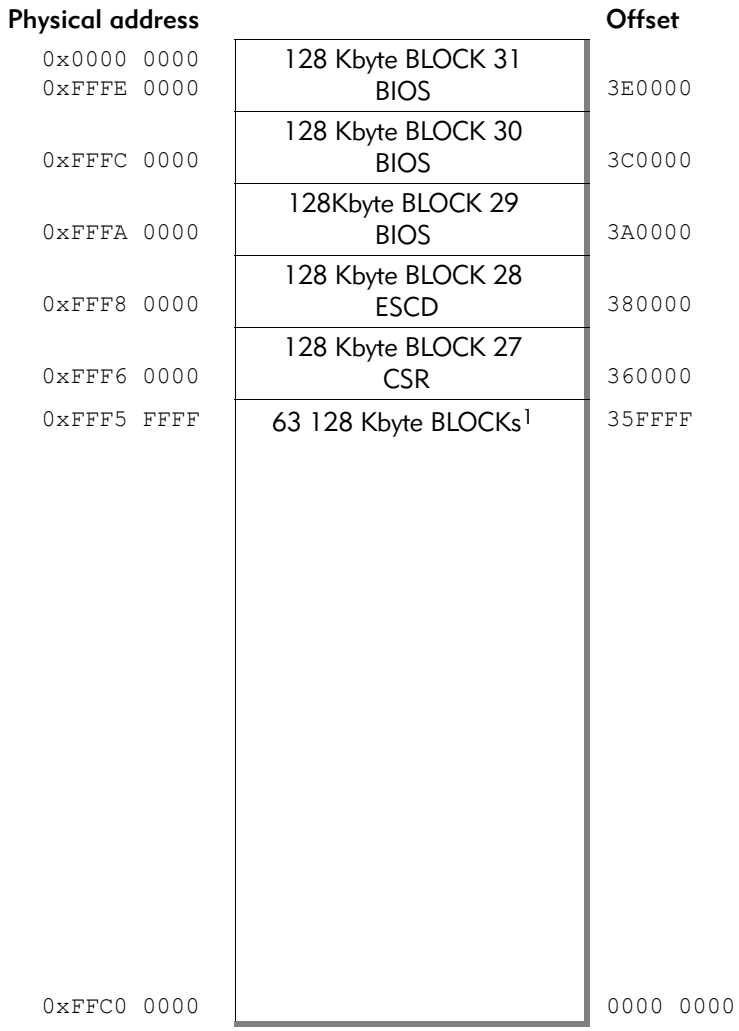
The messages that can display depend upon your system's configuration. For example, systems that do not have a floppy drive will not encounter a situation requiring a diskette error message.

1. Fixed disk errors
   - No drive connected
   - Configured for 0 cylinders
   - Controller reset failed
   - Drive not ready
   - Track 0 seek timed out
   - Drive initialization failed
   - Drive recalibration failed
   - Last track seek failed
2. Video error
   - Color/Mono switch not set correctly
3. Timer error
   - System timer (0) failed
4. Diskette error
   - Floppy type does not match setup
5. I/O chip error
   - I/O conflicts exist for serial and parallel ports, floppy, hard disk (any or all)
6. Other error
   - IRQ conflict, unsupported COM port configuration, keyboard locked
   - Pentium cooling fan has failed
   - The System BIOS *prints* an error message *but does not halt* when it encounters the following error conditions:
     - Configuration error
     - Previous POST execution was incomplete
   - User BIOS Extension Region X exceeds DFFFFh

E Flash memory addresses

The EPC-6315 flash chip contains these major sections:

Figure E-1. Flash chip memory addresses



[1] This area of the flash consists of 63 blocks, each containing

For information about re-programming the flash chip's contents, see *Appendix F, Re-programming the flash chip*.

F Re-programming the flash chip

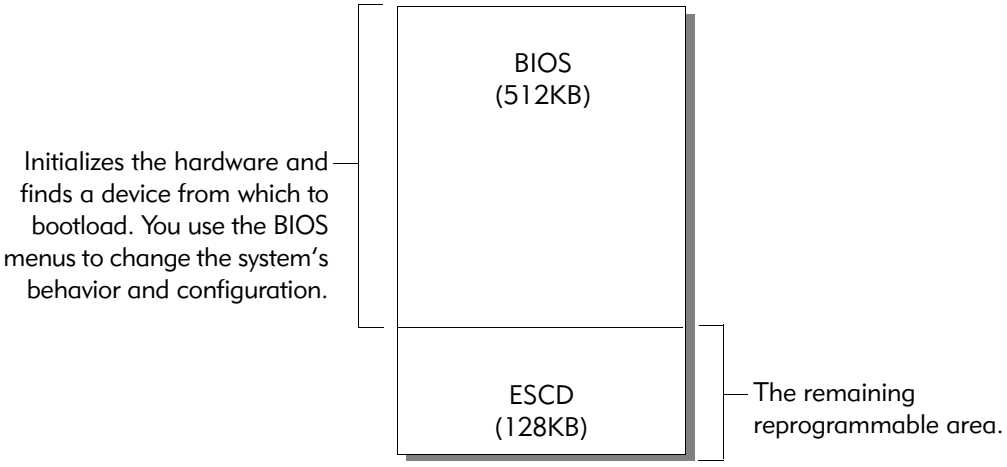
This appendix details how to update or recover your Flash Boot Device (FBD). You accomplish this by re-programming all or part of the EPC-6315's flash chip.

When reading this file online, you can immediately view information about any topic by placing the mouse cursor over a task and clicking.

About the flash chip

The EPC-6315 flash chip contains these major sections:

Figure F-1. Flash chip configuration



About re-programming the flash chip

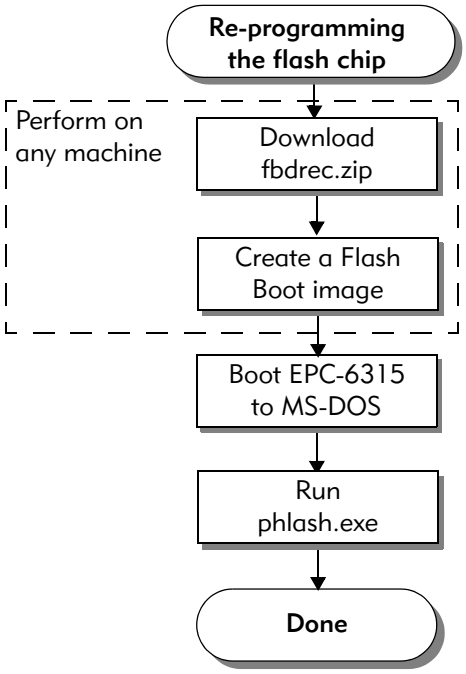
On rare occasions, part or all of the flash chip contents may require replacement.

Use extreme caution when re-programming the flash chip.

You can force re-programming via the phlash program, which re-programs the entire flash chip from a DOS command prompt.

When re-programming the flash chip, follow this process. The rest of this chapter includes detailed instructions for each task:

Figure F-2. Flash chip re-programming process flow



Before you begin

Ensure that you have the following:

- Minimum 2 MB of DRAM to run the re-flash program.
- A 3.5" 1.44 MB hard drive attached to or installed in the system.
- Access to the RadiSys web site.

Creating a Flash Boot diskette

Re-programming the flash chip requires a Flash Boot image that contains both code to perform the task and data to place in the chip.

To create the Flash Boot image on a hard drive:

1. Locate this file from the RadiSys web site and download it to your computer:

   `fbdrec.zip`

2. Unzip the contents to a directory on your hard drive.

   When unzipped, verify that these files required to re-program the flash chip are copied successfully to your hard drive:

Filename	Description
readme.txt	Describes the transmittal and includes instructions and issues that arose too late to include in other documentation
bios.rom	A binary file that contains the BIOS image and Boot Block.
phlash.exe	The program that re-programs the flash chip using data from the other files.
platform.bin	A file that describes the flash chip configuration, and identifies which blocks to erase and re-program.

Using phlash.exe to re-program the flash chip

1. Boot the EPC-6315 into MS-DOS with no memory managers running.
2. Copy the Flash Boot image to the system.

   For detailed information about creating a Flash Boot diskette, see *Before you begin* on page 82.

3. Start the re-programming process. For example:

   ```
   c:\phlash
   ```

   When finished, the phlash program displays a message, then automatically reboots the system.

   If using only console redirection, messages do not display. You must wait approximately three minutes for the reflash to complete.

G Carrier card design

To use Monarch mode, you must design a carrier card that supports Monarch mode. The rest of this appendix provides guidelines for designing such a card.

PrPMC connectors (Jn1 and Jn2)

General

Leave all reserve pins unconnected.

The PCI:~RST signal is an input to the PrPMC. It requires a pullup (1K to +3.3V) for the EPC-6315 to operate properly.

Power

The EPC-6315 includes the following power considerations: +5V, +3.3V, +12V, –12V, and VI/O.

VCC and +3.3V requires:

- A single bulk bypass near the power connection to the EPC-6315.
- A high-frequency decoupling cap at each pin.

+12 and –12V are not used on the board and only require the high-frequency decoupling cap.

VI/O requires a a high-frequency decoupling cap on each pin. VI/O can be either +5V or +3.3V.

PCI

Design interrupt and IDSEL routing to match the *PCI-to-PCI Bridge Architecture Specification Revision 1.1*.

The ~LOCK, ~SDONE, and ~SBO signals are not used; you can leave them unconnected.

Tie JTAG signals to an inactive state. That is, TCK and ~TRST low and TMS and TDI high. Leave TDO unconnected.

Tie ~BUSMODE1 and ~BUSMODE2 through a resistor to VI/O. ~BUSMODE3/NC and ~BUSMODE4/NC can be left unconnected. Although the PrPMC specification requires that these have 10K Ohm pull-down resistors, these are not required for ~BUSMODE3/NC and ~BUSMODE4/NC.

~REQ64 and ~ACK64 should be bussed and tied through a resistor to VI/O.

Jn1

Clocking

The carrier card must provide clocking to the PrPCMC. RadiSys provides an alternative mechanism via Jn4. For more information, see the Jn4 description.

Arbitration

The carrier card must provide arbitration to the PrPCMC. RadiSys provides an alternative mechanism via Jn4. For more information, see the Jn4 description.

Jn2

Processor PMC

M66EN should be bussed and pulled low for 33MHz operation, and high for 66MHz operation.

IDSELB/NC is not used and may be tied low.

Tie Monarch pin low to enable Monarch mode and high to enable non-Monarch mode.

The ~ENUM signal requires a 10K pull-up.

The ~REQ2/NC and ~GNT2/NC pair is not used when implemented on a PrPMC-compliant carrier card. However, you can use these signals to provide arbitration to the rest of the system. For more information, see the Jn4 arbitration section.

The The EPC-6315 does not use the ~RSTOUT/NC signal. However, RadiSys recommends that you bus this signal to all PrPMC sites.

The RadiSys PrPMC does not use the serial interrupt mechanism. However, RadiSys recommends tying ~SERIRQ signal through a resistor to VI/O.

RadiSys-defined PrPMC connector (Jn4)

IDE

RadiSys recommends placing series termination resistors (33.2 Ohms) next to all IDE signals on Jn4, with the exception of the ~IOR, IORDY and ~RST signals. ~IOR should have an AC termination (100 Ohms and 10pF) next to the IDE drive connector on the carrier card. ~IOR should have a series termination resistor (33.2 Ohms) next to the IDE drive connector on the carrier card.

RadiSys recommends adequate bulk and high-frequency decoupling near the IDE drive connector on the carrier card.

Keyboard and mouse

Jn4 provides keyboard and mouse clock and data signals as well as +5V for systems that need to use the EPC-6315's internal keyboard and mouse controller.

Serial port

Jn4 provides all signals needed to implement a full serial port for systems desiring to use the EPC-6315's embedded serial port (COM1).

Clocking

You can use BPCIREF, a PCI output clock, to buffer and provide clocks to the rest of the PCI system on the carrier card. The frequency of this clock is set by the state of the M66EN signal. For more information about this signal, see *Jn2 connector* on page 70.

Arbitration

Jn4 provides four pairs of arbitration signals that you can use in place of an arbiter on the carrier card. Jn2 provides an additional arbitration pair that may be used for the same function as well. For more information, see Table 5-1, *Power-up configuration settings* on page 55.

RTC battery

Jn4 provides PWR_BAT_IN, a connection for the battery. The battery provides backup power to the BIOS CMOS settings for occasions when power is not applied.

UL requires a 1K series resistor. RadiSys recommends isolating this from the +3V power supply with a low-leakage Schottky diode. RadiSys provides this series resistor and a low leakage Schottky resistor on the EPC-6315.

Mechanical and thermal design

The two mounting holes for the front panel are electrically isolated from the rest of the board. The back mounting holes (near Jn1 and Jn4) are connected to logic ground. The reference schematics do not show this properly connected.

Power consumption

The EPC-6315 uses a considerable amount of power from both +5.0V and +3.3V supplies. Ensure that the power supplies on the carrier card can support the full amount of current. Also, when possible, to keep the EPC-6315 as cool as possible, avoid placing high power dissipation components in the vicinity of the PMC.

Airflow

Place the EPC-6315 in a pressurized chassis pushing air across the card. The required airflow should be 200 LFM at the carrier card. Airflow direction should be from the CPU/memory edge to the RadiSys 82600 chipset edge.

Ensure 200 LFM of airflow exists at the leading edge of the heat spreader, regardless of which carrier card PMC slot is used (this indicates no air blockage by other components on the carrier or another PMC).

The carrier card design should accommodate the specific heights of the EPC-6315 components:

- In the I/O region, the the PMC specification limits maximum EPC-6315 component height to 13.5mm.
- In the component region, the maximum component height is 8.2mm.

Of particular interest to designers is that J1 provides user access to the serial port. This 5.7mm tall connector is located where Jn3 normally sits on a carrier card. If this conflict with your carrier card's requirements, contact RadiSys.

Maximum ambient temperature

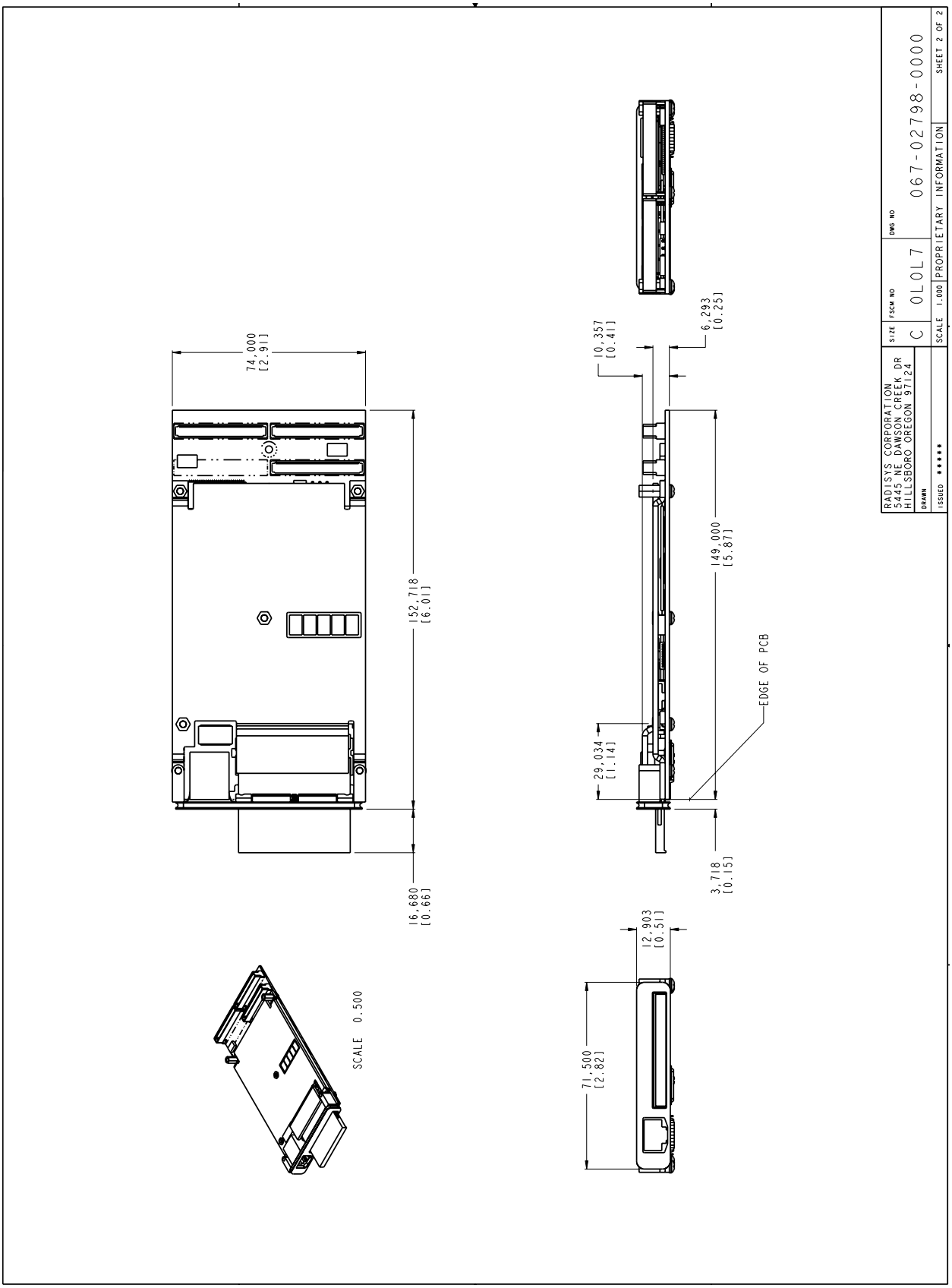
Maximum ambient temperature is 50°C at the EPC-6315.

Carrier card schematic samples

The remainder of this appendix includes sample schematics that you can use as reference when designing a carrier card.

These schematics:

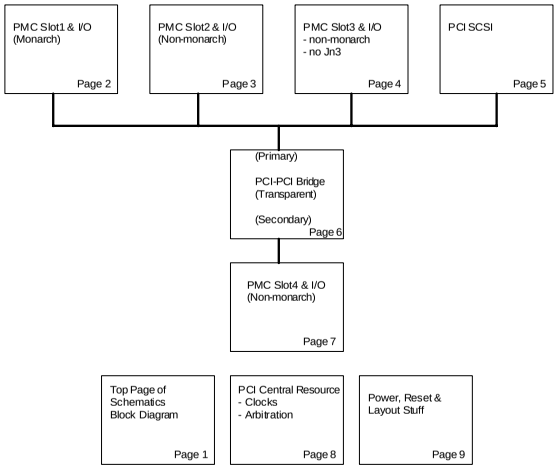
- Include a series resistor and diode between the battery and the Jn4 of the PMC sites; the resistor and diode are not necessary.
- Do not include pull-up resistors on the arbitration signals, located at *sheet 8* on page 97.
- Do not properly show the proper connection between the PMC mounting and keying holes and logic ground.


74,000
[2.91]
152,718
[6.01]
16,680
[0.66]
SCALE 0.500
10,357
[0.41]
6,293
[0.25]
149,000
[5.87]
EDGE OF PCB
29,034
[1.14]
3,718
[0.15]
12,903
[0.51]
71,500
[2.82]
RADISYS CORPORATION
5445 NE DAWSON CREEK DR
HILLSBORO OREGON 97124
SIZE
FSCM NO
C
0L0L7
DWG NO
067-02798-0000
DRAWN
ISSUED *****
SCALE 1.000
PROPRIETARY INFORMATION
SHEET 2 OF 2

HobbitTest

Hardware Engineer: Terry Trausch
Program Manager: Curtis Miller
Customer: RadiSys Factory Test Board

TH-1025-00
060-00729-0000



Revision Notes

Board Revision 00 -> 01 Modifications:
Rev 01 does not exits.

Variant Notes

1. These schematic pages represents the only version.
2. All parts noted DNI (do not install) are not to be included in any bill of materials for any of the variants unless specifically noted below.
3. Add 5 shunts to all BOM's: 40-0039-00.
4. Add 4 batteries to all BOM's: 17-0025-00.

Future Revisions Needed

1. 2.74K pullup resistors to VIO on arbitration signals to all Jn1 signals.
2. Jn4 diode and series resistor should be removed. Connect battery directly to pin.
3. The ground scheme is incorrect at the back of all the PMC sites. It should have NC on the 3.3V and 5V keying holes and GND on the mounting holes nearest Jn1 and Jn3.

This part 060-00729-0000 is used on 061-01456-0000 and may be used on other RadiSys assemblies.

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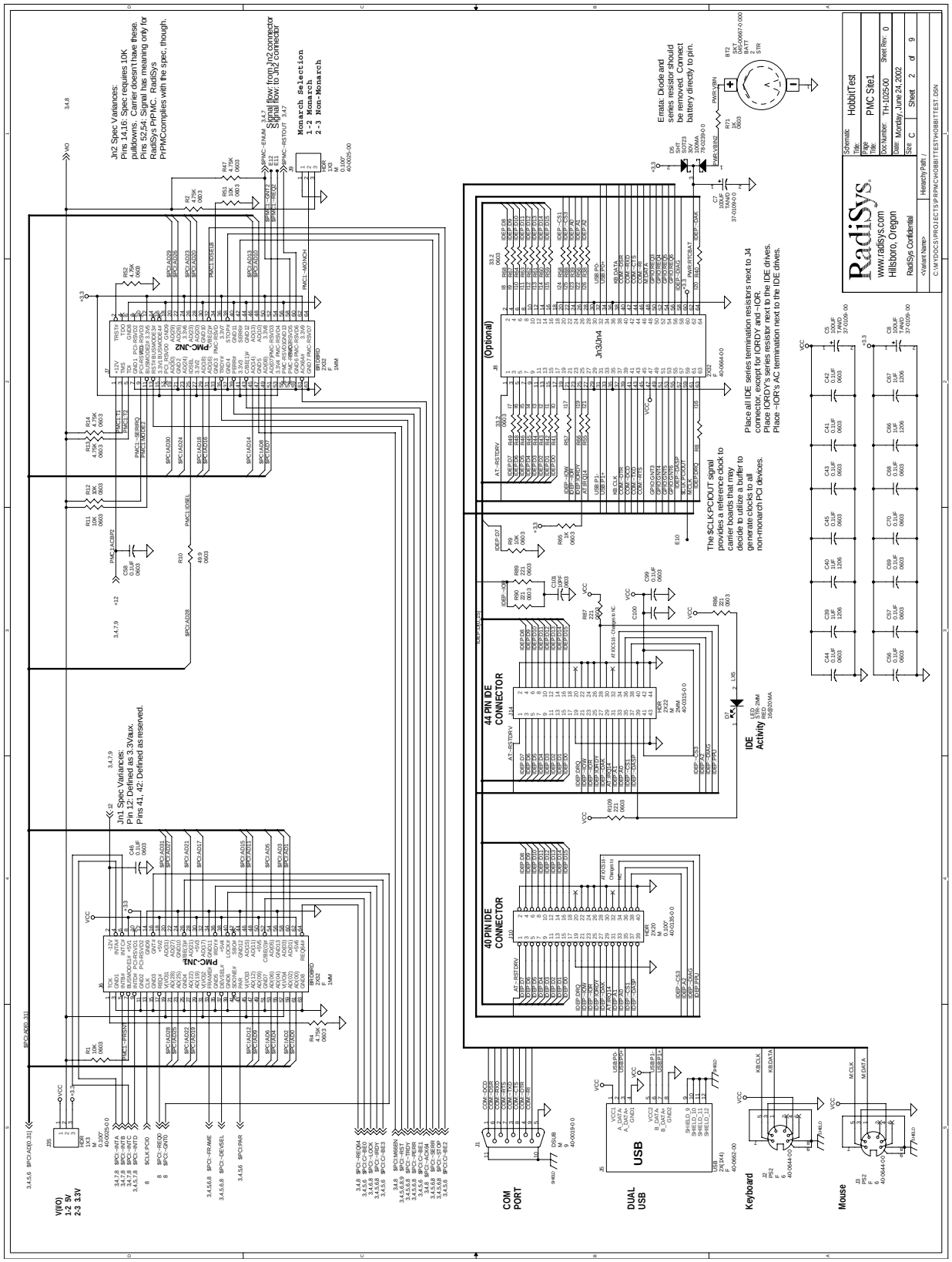
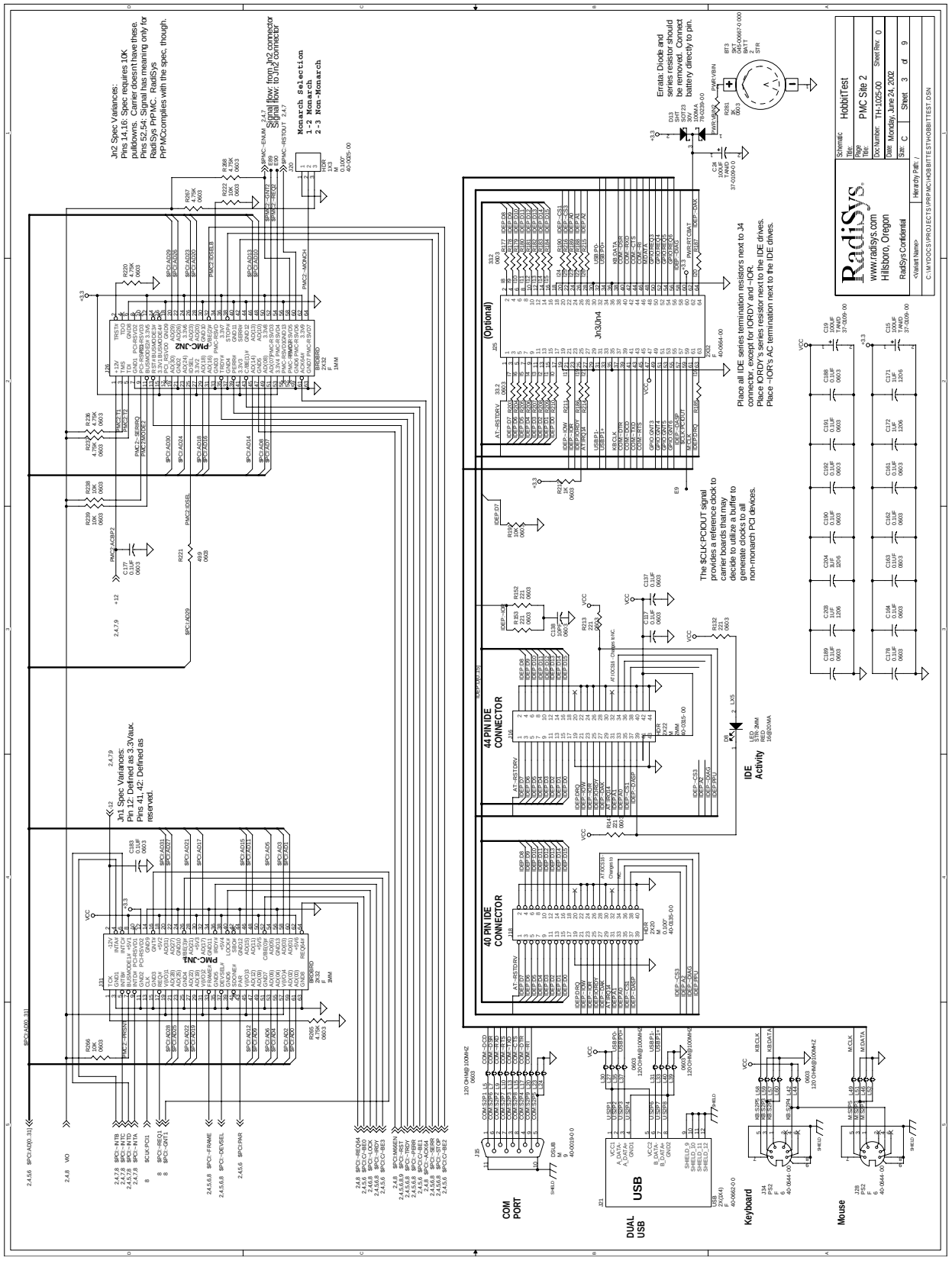
Schematic Title:	HobbitTest
Page Title:	Top Level
Doc Number:	TH-1025-00 Sheet Rev: 0
Date:	Monday, June 24, 2002
Size: C	Sheet 1 of 9
<Variant Name>	Hierarchy Path: /

C:\MYDOCS\PROJECTS\PRPMC\HOBBITTEST\HOBBITTEST.DSN


Jn2 Spec Variances:
Pins 14,16: Spec requires 10K pulldowns. Carrier doesn't have these.
Pins 52,54: Signal has meaning only for RadiSys PrPMC. RadiSys PrPMCcomplies with the spec, though.
Signal flow: from Jn2 connector
Signal flow: to Jn2 connector
Monarch Selection
1-2 Monarch
2-3 Non-Monarch
Jn1 Spec Variances:
Pin 12: Defined as 3.3Vaux.
Pins 41, 42: Defined as reserved.
PMC-JN2
Jn3/Jn4
(Optional)
44 PIN IDE CONNECTOR
40 PIN IDE CONNECTOR
IDE Activity
The SCLK-PCIOUT signal provides a reference clock to carrier boards that may decide to utilize a buffer to generate clocks to all non-monarch PCI devices.
Place all IDE series termination resistors next to J4 connector, except for IORDY and –IOR. Place IORDY's series resistor next to the IDE drives. Place –IOR's AC termination next to the IDE drives.
Errata: Diode and series resistor should be removed. Connect battery directly to pin.
V(I/O) 1-2 5V 2-3 3.3V
COM PORT
DUAL USB
Keyboard
Mouse
RadiSys
www.radisys.com
Hillsboro, Oregon
RadiSys Confidential
Schematic: HobbitTest
Title: PMC Site1
Doc Number: TH-1025-00
Sheet Rev: 0
Date: Monday, June 24, 2002
Size: C
Sheet 2 of 9
C:\MYDOCS\PROJECTS\PRPMC\HOBBIT\TEST\HOBITTEST.DSN


Jn2 Spec Variances:
Pins 14,16: Spec requires 10K pulldowns. Carrier doesn't have these.
Pins 52,54: Signal has meaning only for RadSys PrPMC. RadSys PrPMC complies with the spec, though.
Jn1 Spec Variances:
Pin 12: Defined as 3.3Vaux.
Pins 41, 42: Defined as reserved.
Monarch Selection
1-2 Monarch
2-3 Non-Monarch
Signal flow: from Jn2 connector
Signal flow: to Jn2 connector
Jn3/Jn4
(Optional)
44 PIN IDE CONNECTOR
40 PIN IDE CONNECTOR
IDE Activity
The SCLK-PCIOUT signal provides a reference clock to carrier boards that may decide to utilize a buffer to generate clocks to all non-monarch PCI devices.
Place all IDE series termination resistors next to J4 connector, except for IORDY and -IOR.
Place IORDY's series resistor next to the IDE drives.
Place -IOR's AC termination next to the IDE drives.
Errata: Diode and series resistor should be removed. Connect battery directly to pin.
COM PORT
DUAL USB
Keyboard
Mouse
RadiSys
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RadiSys Confidential
Schematic: HobbitTest
Title: PMC Site 2
Size: C
Doc Number: TH-1025-00
Sheet Rev: 0
Date: Monday, June 24, 2002
Sheet 3 of 9
Hierarchy Path: /
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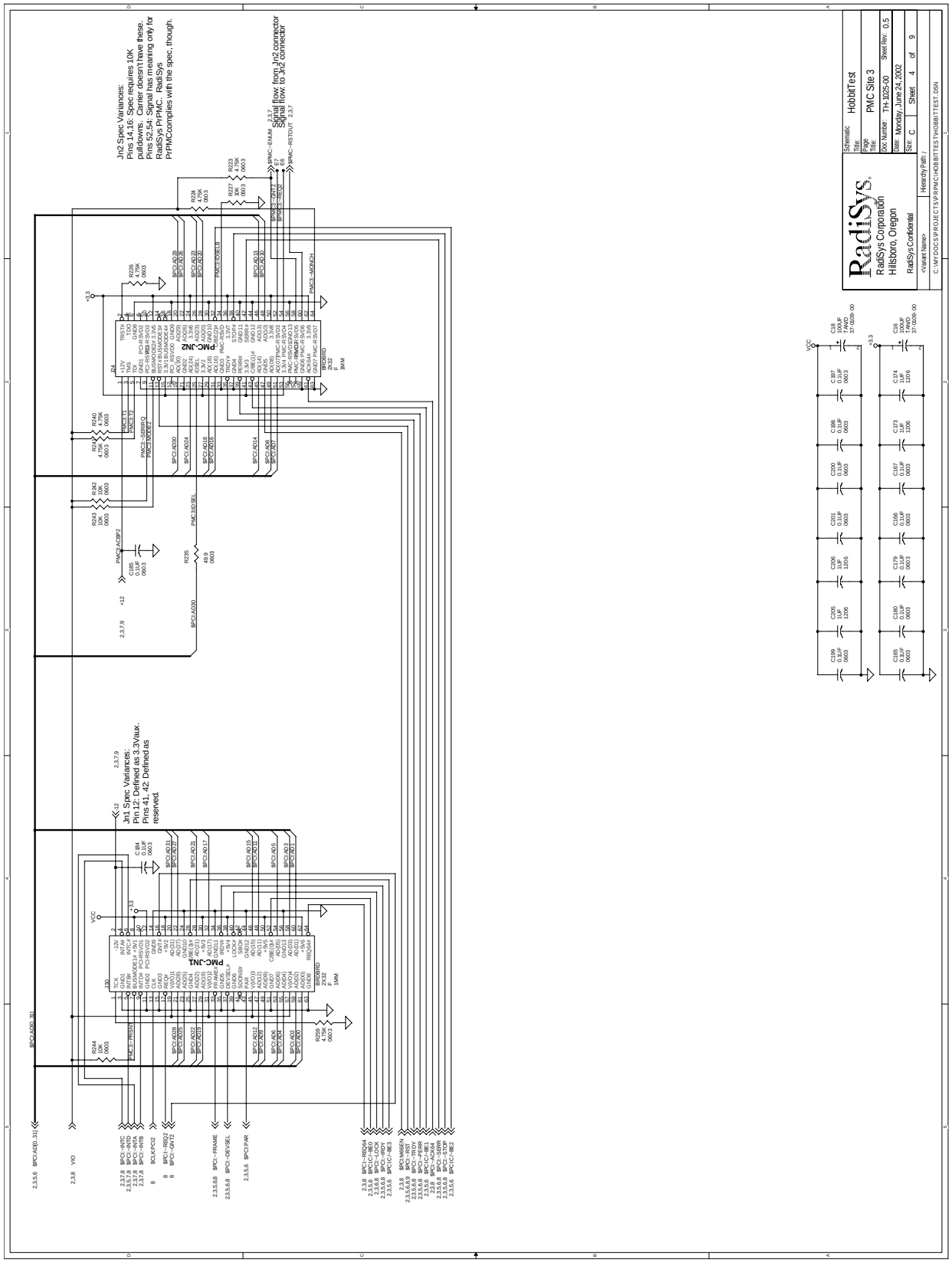
Jn2 Spec Variances:
Pins 44,45: Spec requires 10K pullups. Carrier doesn't have these.
Pins 52,54: Signal has meaning only for RadiSys PrPMC. RadiSys PrPMCcomplies with the spec; though.
Signal flow: from Jn2 connector
Signal flow: to Jn2 connectr
Jn1 Spec Variances:
Pin 12: Defined as 3.3Vaux.
Pins 41, 42: Defined as reserved.
PMC-JN2
PMC-JN1
RadiSys
RadiSys Corporation
Hillsboro, Oregon
RadiSys Confidential
Schematic: HobbitTest
Title:
Page Title: PMC Site 3
Dc Number: TH-1025-00
Sheet Rev: 0.5
Date: Monday, June 24, 2002
Size: C
Sheet 4 of 9
Hierarchy Path:
<Variant Name>
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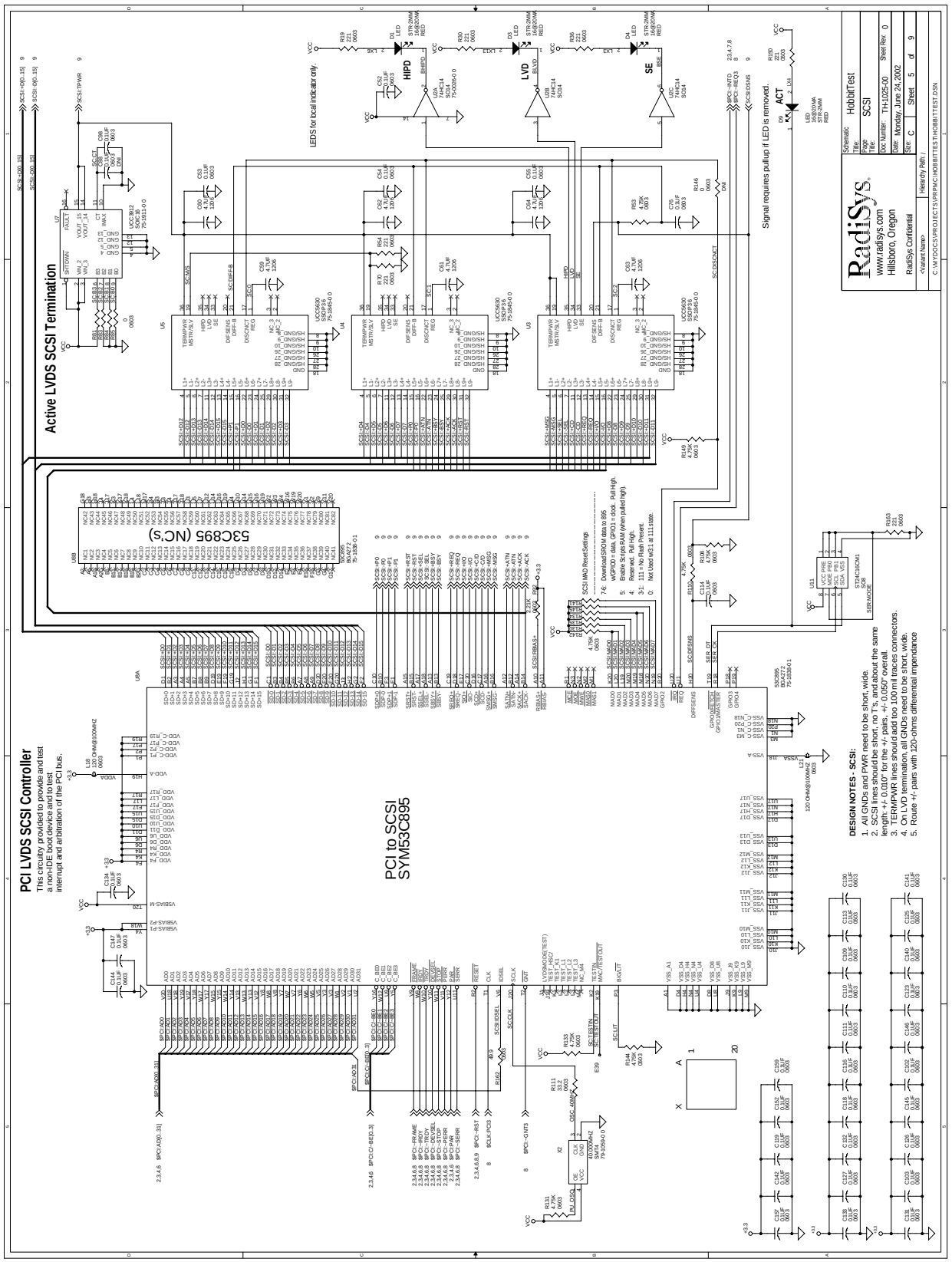
Active LVDS SCSI Termination
PCI LVDS SCSI Controller
This circuitry provided to provide and test a non-IDE boot device and to test interrupt and arbitration of the PCI bus.
PCI to SCSI SYM53C895
53C895 (NC's)
LEDs for bcal indicator only.
Signal requires pullup if LED is removed.
HIPD
LVD
SE
ACT
DESIGN NOTES - SCSI:
1. All GNDs and PWR need to be short, wide.
2. SCSI lines should be short, no T's, and about the same length +/- 0.010" for the +/- pairs, +/- 0.050" overall.
3. TERMPWR lines should add too 100 mil traces connectors.
4. On LVD termination, all GNDs need to be short, wide.
5. Route +/- pairs with 120-ohms differential impedance
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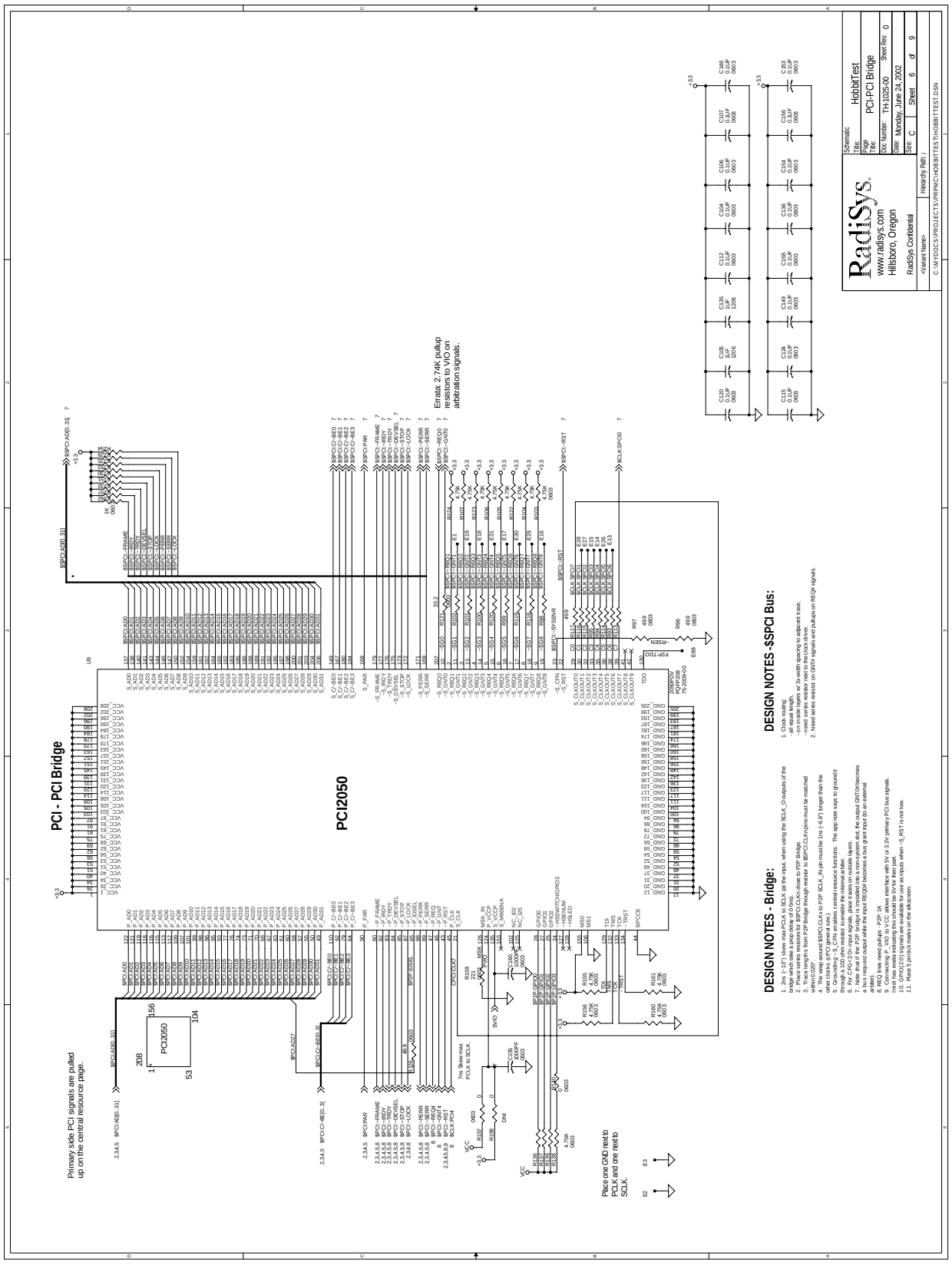
Hillsboro, Oregon
RadiSys Confidential
HobbitTest
SCSI
TH-1025-00
Monday, June 24, 2002


PCI - PCI Bridge
PCI2050
Primary side PCI signals are pulled up on the central resource page.
Errata: 2.74K pullup resistors to VIO on arbitration signals.
DESIGN NOTES - Bridge:
DESIGN NOTES -$PCI Bus:
Place one GND next to PCLK and one next to SCLK.
RadiSys
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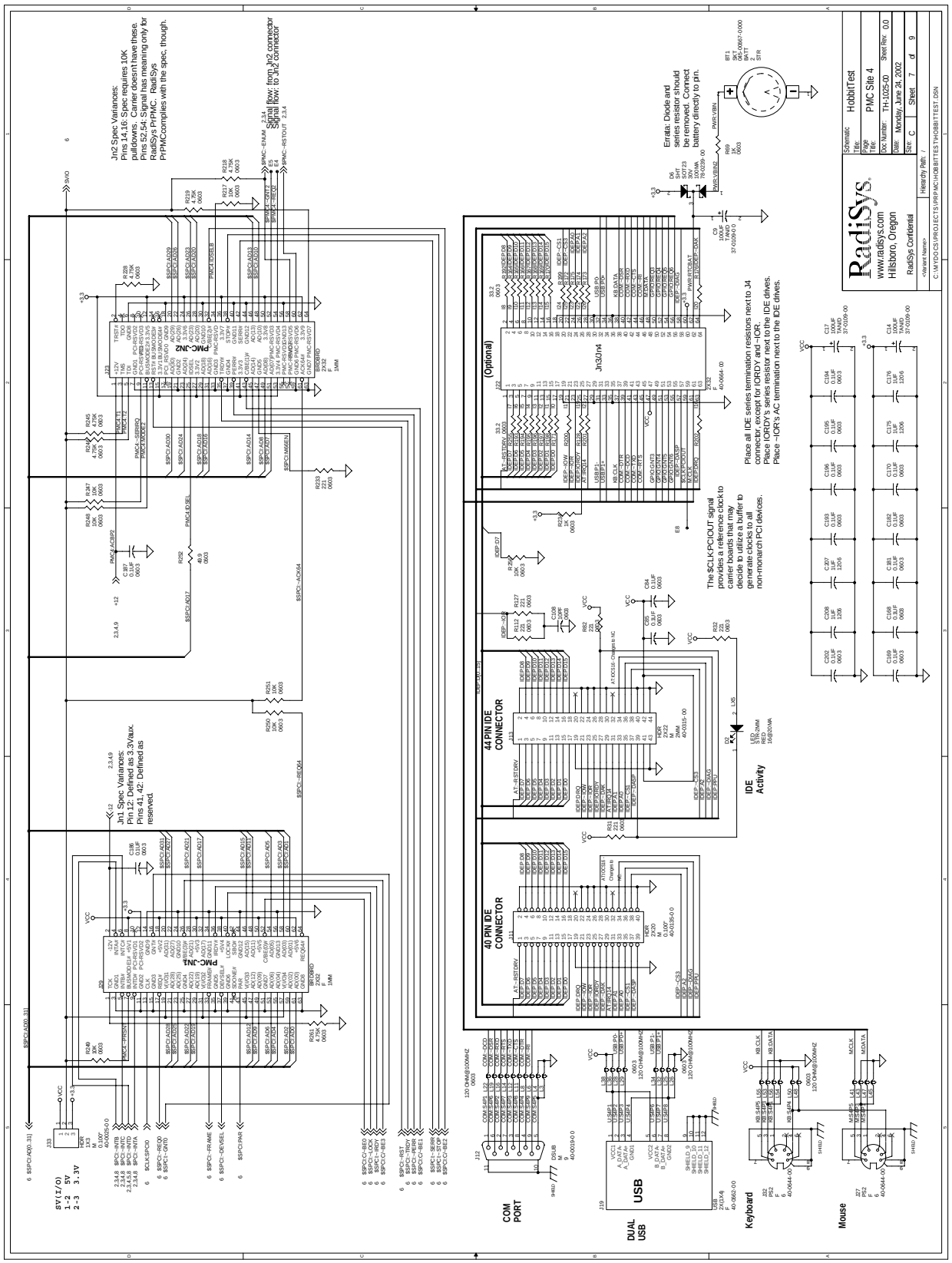
Hillsboro, Oregon
HobbitTest
PCI-PCI Bridge
TH-1025-00
Monday, June 24, 2002
RadiSys Confidential


Jn2 Spec Variances:
Pins 14.16: Spec requires 10K pulldowns. Carrier doesn't have these.
Pins 52,54: Signal has meaning only for RadiSys PrPMC. RadiSys PrPMCcompiles with the spec, though.
Signal flow: from Jn2 connector
Signal flow: to Jn2 connector
Jn1 Spec Variances:
Pin 12J: Defined as 3.3Vaux.
Pins 41,42: Defined as reserved.
Jn3/Jn4
(Optional)
44 PIN IDE CONNECTOR
40 PIN IDE CONNECTOR
IDE Activity
The $CLKPCIOUT signal provides a reference clock to carrier boards that may decide to utilize a buffer to generate clocks to all non-monarch PCI devices.
Place all IDE series termination resistors next to J4 connector, except for IORDY and –IOR:
Place IORDY's series resistor next to the IDE drives.
Place –IOR's AC termination next to the IDE drives.
Errata: Diode and series resistor should be removed. Connect battery directly to pin.
COM PORT
DUAL USB
Keyboard
Mouse
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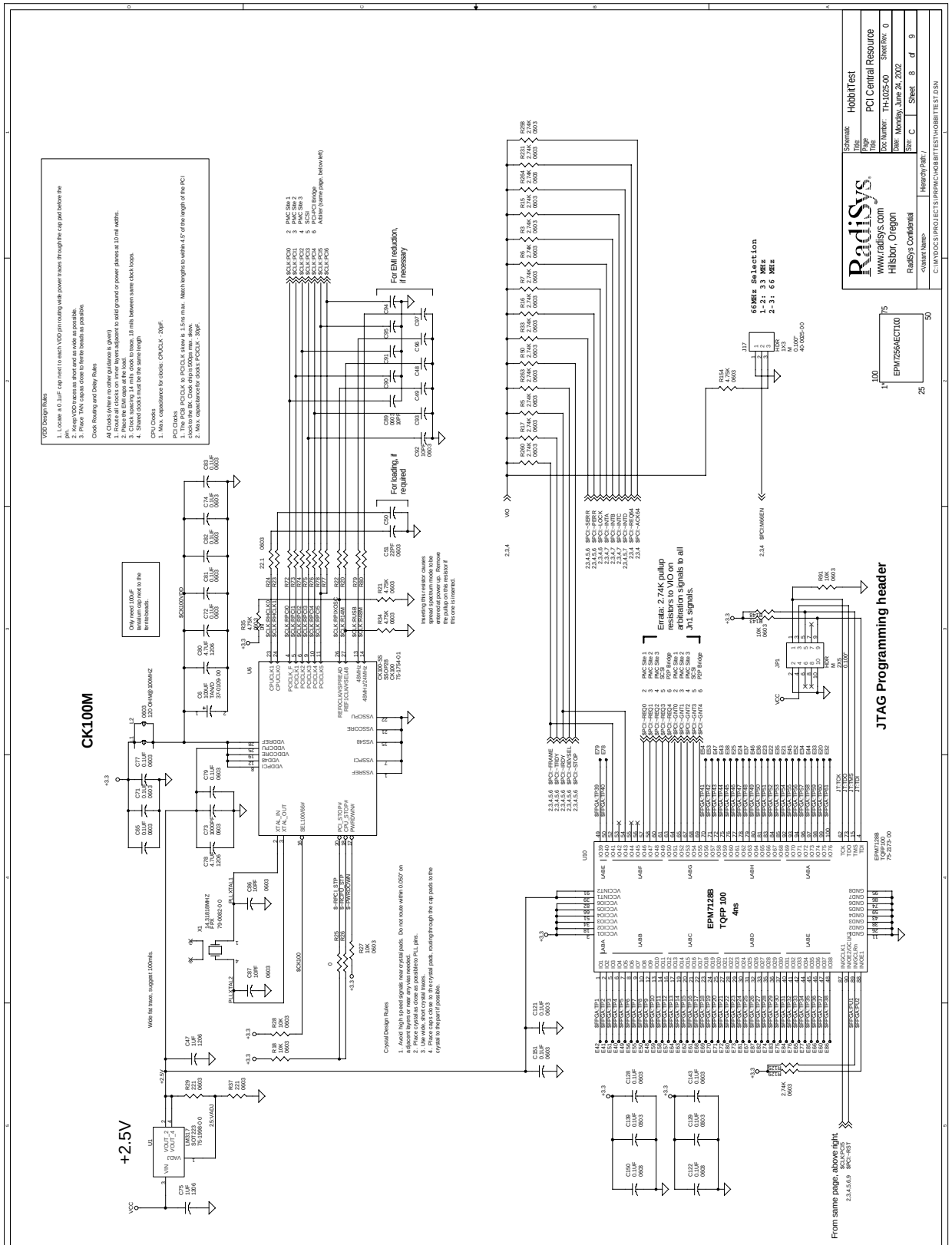
HobbitTest
PMC Site 4
TH-1025-00
Monday, June 24, 2002


CK100M
+2.5V
JTAG Programming header
Errata: 2.74K pullup resistors to VIO on arbitration signals to all Jn1 signals.
66MHz Selection
1-2: 33 MHz
2-3: 66 MHz
EPM7128B TQFP 100 4ns
EPM7256AETI100
RadiSys
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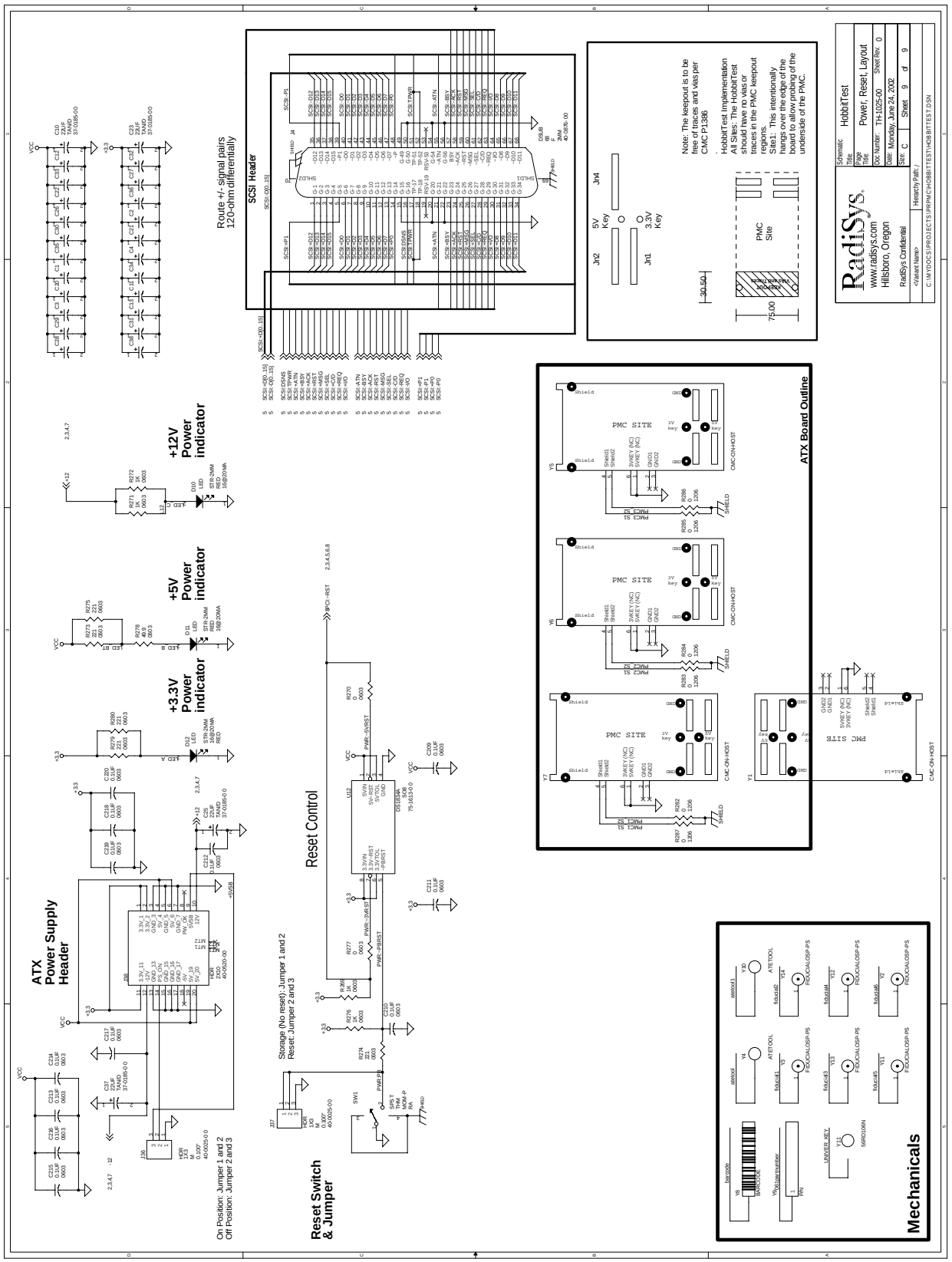
Hillsboro, Oregon
Schematic: HobbitTest
Page Title: PCI Central Resource
Doc Number: TH-1025-00
Sheet Rev: 0
Date: Monday, June 24, 2002
Size: C
Sheet 8 of 9
RadiSys Confidential
C:\MYDOCS\PROJECTS\PRPMC\HOBBIT\TEST\HOBBITTEST.DSN


SCSI Header
Route +/- signal pairs
120-ohm differentially
Reset Control
Reset Switch
& Jumper
ATX
Power Supply
Header
+3.3V
Power
indicator
+5V
Power
indicator
+12V
Power
indicator
ATX Board Outline
PMC SITE
CMC-ON-HOST
Mechanicals
Note: The keepout is to be free of traces and vias per CMC P1386
HobbitTest Implementation All Sites: The HobbitTest should have no vias or traces in the PMC keepout region. Site1: This intentionally hangs over the edge of the board to allow probing of the underside of the PMC.
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HobbitTest
Power, Reset, Layout
Sheet 9 of 9

H EPC-6315 test board

The EPC-6315 test board (hereafter, Test Board) is a full ATX-sized, four PMC site circuit board that you can use to begin production, test, and early development using the RadiSys EPC-6315 PrPMC.

This product assumes an intimate knowledge of the PrPMC specification, the standards governing other external interfaces to the PrPMC, and basic computer knowledge.

Features

Four 32-bit PMC sites with onboard arbitration, power reset, and clock selection of 33MHz or 66 MHz.

Feature	Description
Sites 1 and 2	• Clock speeds of 33MHz or 66MHz. • Monarch or non-Monarch selection between sites 1 and 2. • Keyboard, mouse, serial port (DB9), IDE (40 and 44 pin), and battery interfaces. • PMC standard Jn1, Jn2, and Jn4 connectors.
Site 3	• Clock speeds of 33MHz or 66MHz. • Non-Monarch site. • PMC standard Jn1 and Jn2 interfaces (no Jn4 interface).
LSI 53C895 SCSI Controller	• SCSI active termination. • Industry standard 68ppin SCSI connector. • 33MHz operation only.
PCI-PCI bridge	• Provides a PMC site behind a 33MHz bridge. • 33MHz operation only. • Independent primary and secondary side V I/O selection between 5V and 3.3V.
Site 4	• Clock speed of 33Hz. • Non-Monarch site. • Keyboard, mouse, serial port (DB9), IDE (40 and 44 pin), and battery interfaces. • PMC standard Jn1, Jn2, and Jn4 connectors.
ATX style power connector, power indicator LEDS and 3 pin power on/off jumper.	
Pushbutton and jumper resets.	

External interfaces

The Test Board, being a piece of lab equipment, has several connectors and jumpers available for use. The function of each connector is noted below.

Site(s)	No.	Connector
—	1	ATX power connector.
—	1	ATX 3-pin power on/off jumper.
1, 2, 4	2 ea	Industry standard 40- and 44-pin IDE connectors.
1, 2, 4	1 ea	DB9 serial port with full modem signals.
1, 2, 4	2 ea	6-pin mini-DIN keyboard and mouse connectors.
1, 2, 4	1	Battery in a socket (sites 1, 2, and 4).
—	2	3-pin jumpers for primary and secondary V I/O voltage selections (+5V or +3.3V).
—	1	3-pin jumper for clock speed selection (33MHz or 66MHz). Selecting 66MHz automatically disables SCSI, PCI-to-PCI bridge, and Site 4.
1, 2	2	3-pin jumpers for Monarch or non-Monarch selection.
—	1	Pushbutton switch and one three pin jumper for reset.
—	1	3-pin jumper for arbitration selection. **Note**: This feature does not operate. The only available arbitration selection is that the Test Board provides arbitration. If this presents a problem, contact RadiSys as described in *Where to get more information* on page iv.

Specifications

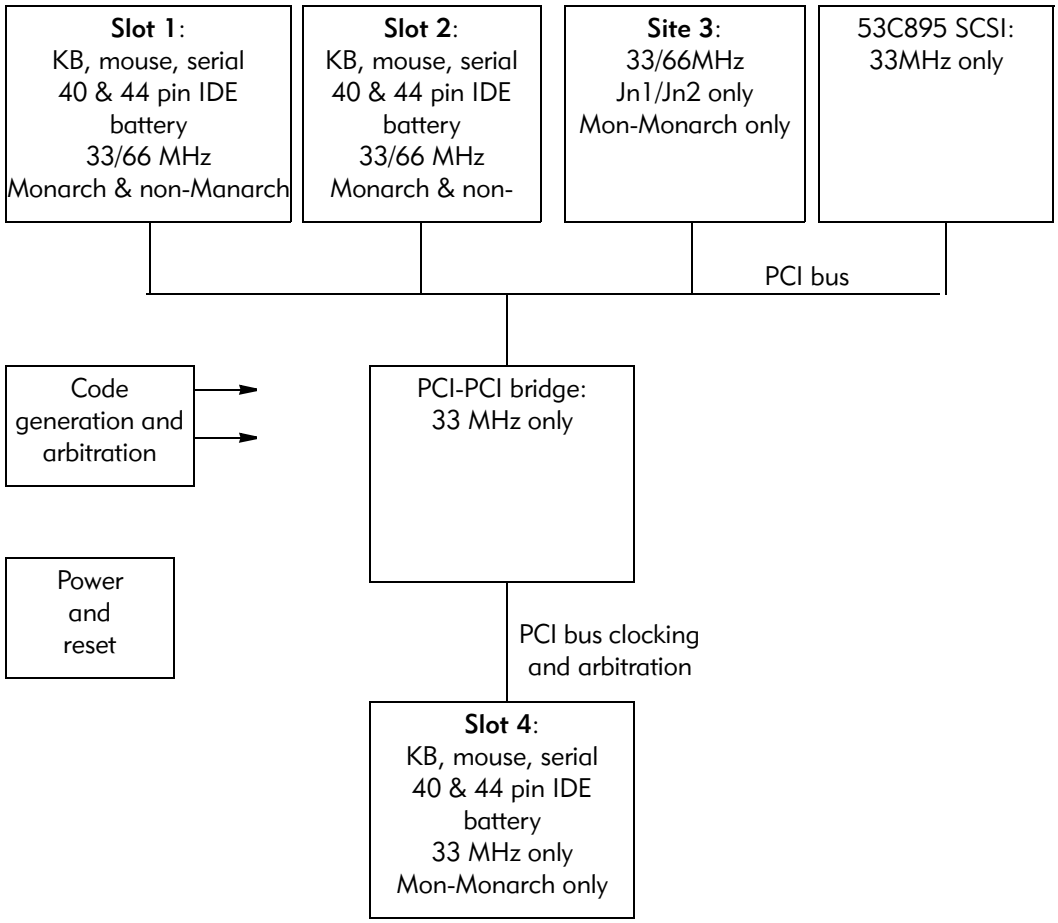
The Test Board is not intended to meet any specific environmental specifications. As the board is typically used in an engineering lab environment where proper ESD procedures are followed, EMC is not considered an issue. It is assumed that the operating temperature is 20°C to 30°C, and humidity is 30% to 50%.

Table H-1. Environmental specifications

Characteristic	Value
Dimensions	Full-size ATX board
Board thickness	2mm

Block diagram

Figure H-1. Block diagram



Physical interfaces

The keyboard, mouse, serial port, and IDE connectors are all common industry standard pinouts.

Connectors and jumpers

The following table contains the list of all connectors and jumpers on the board and a description for each jumper.

Table H-2. Connector and jumper descriptions

Item	Description
J43	ATX power connector (industry standard pinout)
J39	ATX power on/off jumper (1–2 on, 2–3 off)
J13, J12, J?	40 pin IDE connector (industry standard pinout)
J15, J17, J?	44 pin IDE connector (industry standard pinout)
J14, J1, J18	Serial port (industry standard pinout)

Table H-2. Connector and jumper descriptions

J30, J3, J31	Mouse (industry standard pinout)
J35, J2, J37	Keyboard (industry standard pinout)
J36	Secondary PCI bus V I/O (1–2 +5V, 2–3 +3.3V)
J16	Artbiter select (Does not function)
SW1	Pushbutton reset
JP1	(RadiSys only)
J40	Reset (1–2 reset, 2–3 no reset)
J38	Primary PCI bus V I/O (1–2 +5V, 2–3 +3.3V)
J20	PCI Bus clock select 1–2 33MHz, 2–3 66MHz
J41, J?	Monarch – non Monarch selection (1–2 Monarch, 2–3 non-Monarch)

Reset switch

SW1 is a reset pushbutton switch. Pressing it results in a reset of all PMC sites. Connecting pins 1 and 2 of J40 has the same effect.

Interrrupts

Table H-3. PCI device configuration

Peripheral	IDSEL	Bus	INT	Arbitration
Site1	AD28	0	A	0
Site 2	AD29	0	B	1
Site 3	AD30	0	C	2
SCSI	AD31	0	D	3
PCI bridge	AD27	0, 1	–	4
Site 4	AD17	1	B	From PCI bridge

Glossary

access time A factor in measurement of a memory storage device's operating speed. It is the amount of time required to perform a read operation. More specifically, it is the period of time between which the memory receives a read command signal and the time when the requested data becomes available to the system data bus.

address A number that identifies the location of a word in memory. Each word in a memory storage device or system has a unique address. Addresses are always specified as a binary number, although octal, hexadecimal, and decimal numbers are often used for convenience.

ANSI (American National Standards Institute) An organization dedicated to advancement of national standards related to product manufacturing.

APM 1.1 (Advanced Power Management) A software interface specification that allows operating system device drivers to control the power management functionality of a PC.

ATA (AT Bus Attachment) An interface definition for PC peripherals. See *IDE*.

Autotype A convenient method of IDE device detection whereby the system BIOS queries the IDE device to obtain operational parameters. If the device supports autotype, this information is passed to the BIOS where it is used to automatically configure the drive controller.

BDA (BIOS Data Area) BIOS Data Area. A 256 byte block of DRAM starting at address 400H that contains data initialized and used by the System BIOS detailing the system configuration and errors encountered during POST.

BIOS (Basic Input/Output System) Firmware in a PC-compatible computer that runs when the computer is powered up. The BIOS initializes the computer hardware, allows the user to configure the hardware, boots the operating system, and provides standard mechanisms that the operating system can use to access the PC's peripheral devices.

BIOS extension An object code module that is typically integrated into the FBD or placed into a ROM that is accessible on the peripheral bus (PCI, ISA, etc.) in the address range 0C0000h through 0DFFFFh. BIOS extensions have a pre-defined header format and contain code that is used to extend the capabilities of the System BIOS.

BIOS image Information contained in the flash boot device in binary file format consisting of initialzation data, setup configuration data, diagnostic sequences, and other instructions necessary to start up a computer and prepare it to load an operating system.

Brecovery A process whereby an existing, corrupt BIOS image in the flash boot device is overwritten with a new image. Also referred to as a flash recovery. The EPC-6315 does not support this feature.

BIOS update	A process whereby an existing, uncorrupted BIOS image in the flash boot device is overwritten with a new image. Also referred to as a flash update.
bit	A binary digit.
boot	The process of starting a computer and loading the operating system from a powered down state (cold boot) or after a computer reset (warm boot). Before the operating system loads, the computer performs a general hardware initialization and resets internal registers.
boot device	The storage device from which the computer boots the operating system.
boot sequence	The order in which a computer searches external storage devices for an operating system to boot. The boot device must be the first in the boot sequence.
byte	A group of 8 bits.
CAS	(Column Address Strobe) An input signal from the DRAM controller to an internal DRAM latch register specifying the column at which to read or write data. The DRAM requires a column address and a row address to define a memory address. Since both parts of the address are applied at the same DRAM inputs, use of column addresses and row addresses in a multiplexed array allows use of half as many pins to define an address location in a DRAM device as would otherwise be required.
chipset	One or more integrated circuits that, along with a CPU, memory, and other peripherals, implements an IBM PC-AT compatible computer. The chipset typically implements a DRAM controller, bus, interface logic, and PC peripheral devices.
CHS	(Cylinders/Heads/Sectors) A specification of disk drive operating parameters consisting of the number of disk cylinders, disk drive read/write heads, and disk sectors.
CMOS	(Complimentary Metal Oxide Semiconductor) A fast, low power semiconductor RAM used to store system configuration data.
COM port	A bi-directional serial communication port which implements the RS-232 specification.
conventional memory	The first 640 KB of a computer's total memory capacity. If a computer has no extended memory, conventional memory equals the total memory capacity. In typical computer systems, conventional memory can contain BIOS data, the operating system, applications, application data, and terminate and stay resident (TSR) programs. Also called system memory.
CPU	(Central Processing Unit) A semiconductor device which performs the processing of data in a computer. The CPU, also referred to as the microprocessor, consists of an arithmetic/logic unit to perform the data processing, and a control unit which provides timing and control signals necessary to execute instructions in a program.
CSR	(CMOS Save and Restore) A System BIOS feature that allows the user to backup the contents of CMOS RAM (contained within the real time clock) to the BIOS Flash device to be restored later if necessary (such as when the real time clock battery dies).
default	The state of all user-changeable hardware and software settings as they are originally configured before any changes are made.

DIP (Dual In-Line Package) A semiconductor package configuration consisting of a rectangular plastic case with two rows of pins, one row on each lengthwise side.

DOS (Disk Operating System) One or more programs which allow a computer to use a disk drive as an external storage device. These programs manage storage and retrieval of data to and from the disk and interpret commands from the computer operator.

DRAM. (Dynamic Random Access Memory) Semiconductor RAM memory devices in which the stored data does not remain permanently stored, even with the power applied, unless the data are periodically rewritten into memory during a refresh operation.

driver A software component of the operating system which directs the computer interface with a hardware device. The software interface to the driver is standardized such that application software calling the driver requires no specific operational information about the hardware device.

ECP (Extended Capabilities Port) An enhancement of the standard PC parallel port that allows high speed bi-directional data transfers and other features.

EDO (Extended Data Out) A type of DRAM that allows higher memory system performance since the data pins are still driven when CAS# is de-asserted. This allows the next DRAM address to be presented to the device sooner than with Fast Page Mode DRAM.

EEPROM (Electrically Erasable Programmable ROM) Specifically, those EPROMs which may be erased electrically as compared to other erasing methods.

error checking and correction A feature of the T2 chipset that enables it to detect single or multi-bit errors in DRAM reads and correct single bit errors. This feature requires that all banks of DRAM use x36 (parity) SO DIMMs.

ESCD (Extended System Configuration Data) A block of nonvolatile memory that stores information on the devices found and configured by the Plug and Play BIOS.

extended memory The RAM address space, in a computer so equipped, above the 1 MB level.

external device A peripheral or other device connected to the computer from an external location via an interface cable.

FBD (Flash Boot Device) A flash memory device containing the computer's BIOS. In the EPC-6315, a 4 MByte Intel 28F320J3A semiconductor flash memory containing the system BIOS images, the BIOS initializing code.

fixed disk A hard disk drive or other data storage device having no removable storage medium. Fixed disk storage devices use inflexible disk media and are sealed to prevent data loss due to media surface contamination. Fixed disks generally provide the most storage space for a given cost when compared to semiconductor, tape, and other popular mass storage technologies.

Flash memory A fast EEPROM semiconductor memory typically used to store firmware such as the computer BIOS. Flash memory also finds general application where a semiconductor non-volatile storage device is required.

Flash recovery	See *Brecovery*.
Flash update	See *BIOS update*.
force update	See *Brecovery*.
FPGA	(Field Programmable Gate Array) A large, general-purpose logic device that is programmed at power-up to perform specific logic functions.
FPM	(Fast Page Mode) A "standard" type of DRAM that is lower performance than EDO.
GB or GByte	(Gigabyte) Approximately one billion (US) or one thousand million (Great Britain) bytes. 2^30 = 1,073,741,824 bytes exactly.
h	(Hexadecimal) A base-16 numbering system using numeric symbols 0 through 9 plus alpha characters A, B, C, D, E, and F as the 16 digit symbols. Digits A through F are equivalent to the decimal values 10 through 15.
hang	A condition where the system microprocessor suspends processing operations due to an anomaly in the data or an illegal instruction.
header	A mechanical pin and sleeve style connector on a circuit board. The header may exist in either a male or female configuration. For example, a male header has a number and pattern of pins which corresponds to the number and pattern of sleeves on a female header plug.
host bus	The address/data bus that connects the CPU and the chipset.
I/O	(Input/Output) The communication interface between system components and between the system and connected peripherals.
IDE	(Integrated Drive Electronics) A hard disk drive/controller interface standard. IDE drives contain the controller circuitry at the drive itself, as compared to the location of this circuitry on the computer motherboard in non-IDE systems. IDE drives typically connect to the system bus with a simple adapter card containing a minimum of on-board logic.
INT	(Interrupt Request) A software-generated interrupt request.
IRDA or IrDA	(Infra-red Data Association) A specification for high-speed data communication using infrared drivers and receivers for short-range wireless data transmission.
IRQ	(Interrupt Request) In ISAbus systems, a microprocessor input from the control bus used by I/O devices to interrupt execution of the current program and cause the microprocessor to jump to a special program called the interrupt service routine. The microprocessor executes this special program, which normally involves servicing the interrupting device. When the interrupt service routine is completed, the microprocessor resumes execution of the program it was working on before the interruption occurred.
ISA	(Industry Standard Architecture) A popular microcomputer expansion bus architecture standard. The ISA standard originated with the IBM PC when the system bus was expanded to accept peripheral cards.

ISR	(Interrupt Service Routine) A program executed by the microprocessor upon receipt of an interrupt request from an I/O device and containing instructions for servicing of the device.
jumper	A set of male connector pins on a circuit board over which can be placed coupling devices to electrically connect pairs of the pins. By electrically connecting different pins, a circuit board can be configured to function in predictable ways to suit different applications.
KB or KByte	(Kilobyte) Approximately one thousand bytes. 2^{10} = 1024 bytes exactly.
LBA	(Logical Block Addressing) A method the system BIOS uses to reference hard disk data as logical blocks, with each block having a specific location on the disk. LBA differs from the CHS reference method in that the BIOS requires no information relating to disk cylinders, heads, or sectors. LBA can be used only on hard disk drives designed to support it.
logical address	The memory-mapped location of a segment after application of the address offset to the physical address.
MB or MByte	(Megabyte) Approximately one million bytes. 2^20 = 1,048,576 bytes exactly.
memory	A designated system area to which data can be stored and from which data can be retrieved. A typical computer system has more than one memory area. See *conventional memory* and *extended memory*.
memory shadowing	Copying information from an extension ROM into DRAM and accessing it in this alternate memory location.
Monarch mode	A Processor PMC that acts as the main processing element. In this mode, the PPMC performs PCI bus enumeration at power-up and handles interrupts from devices requesting service. A system can have only one PPMC operating in Monarch mode. See *non-Monarch mode*.
non-Monarch mode	A secondary CPU that is not a main CPU, does not perform PCI bus enumeration, and may generate interrupts to the main CPU. A system can have as many non-Monarch PPMCs as the electrical interface capacity on the carrier card allows. See *Monarch mode*.
offset	The difference in location of memory-mapped data between the physical address and the logical address.
operating system	See *DOS*.
PAL	(Programmable Array Logic) A semiconductor programmable ROM which accepts customized logic gate programming to produce a desired sum-of-products output function.
PC/AT	(Personal Computer/Advanced Technology) A popular computer design first introduced by IBM in the early 1980s.
PCI	(Peripheral Connect Interface) A popular microcomputer bus architecture standard.
peripheral device	An external device connected to the system for the purpose of transferring data into or out of the system.

physical address The address or location in memory where data is stored before it is moved as memory remapping occurs. The physical address is that which appears on the computer's address bus when the CPU requests data from a memory address. When remapping occurs, the data can be moved to a different memory location or logical address.

pinout A diagram or table describing the location and function of pins on an electrical connector.

PMC (PCI Mezzanine Card) A new standard form factor for PCI add-in modules. PMCs mate with their respective connectors on the motherboard and are secured with screws.

PLL (Phase-Locked Loop) A semiconductor device which functions as an electronic feedback control system to maintain a closely regulated output frequency from an unregulated input frequency. The typical PLL consists of an internal phase comparator or detector, a low pass filter, and a voltage controlled oscillator which function together to capture and lock onto an input frequency. When locked onto the input frequency, the PLL can maintain a stable, regulated output frequency (within bounds) despite frequency variance at the input.

POST (Power On Self Test) A diagnostic routine which a computer runs at power up. Along with other testing functions, this comprehensive test initializes the system chipset and hardware, resets registers and flags, performs ROM checksums, and checks disk drive devices and the keyboard interface.

PQFP (Plastic Quad Flat Pack) A popular package design for integrated circuits of high complexity.

program A set of instructions a computer follows to perform specific functions relative to user need or system requirements. In a broad sense, a program is also referred to as a software application, which can actually contain many related, individual programs.

PS/2 (Personal System 2) Computers designed with IBM's proprietary bus architecture known as Micro Channel.

PSB Processor Side Bus.

RAM (Random Access Memory) Memory in which the actual physical location of a memory word has no effect on how long it takes to read from or write to that location. In other words, the access time is the same for any address in memory. Most semiconductor memories are RAM.

RAS (Row Address Strobe) An input signal to an internal DRAM latch register specifying the row at which to read or write data. The DRAM requires a row address and a column address to define a memory address. Since both parts of the address are applied at the same DRAM inputs, use of row addresses and column addresses in a multiplexed array allows use of half as many pins to define an address location in a DRAM device as would otherwise be required.

real mode The operational mode of Intelx86 CPUs that uses a segmented, offset memory addressing method. These CPUs can address 1 MB of memory using real mode.

real mode address A memory address composed of two 16-bit values: a segment address and an offset quantity. A real mode address is constructed by shifting a segment address 4 bits to the left and then adding the offset value. A real mode address is a physical address.

reflashing	The process of replacing a BIOS image, in binary format, in the flash boot device.
register	An area typically inside the microprocessor where data, addresses, instruction codes, and information on the status on various microprocessor operations are stored. Different types of registers store different types of information.
reset	A signal delivered to the microprocessor by the control bus, which causes a halt to internal processing and resets most CPU registers to 0. The CPU then jumps to a starting address vector to begin the boot process.
RFA	(Resident Flash Array) The RFA represents flash memory that is resident on the hardware platform that is utilized for OS or application purposes.
ROM	(Read Only Memory) A broad class of semiconductor memories designed for applications where the ratio of read operations to write operations is very high. Technically, a ROM can be written to (programmed) only once, and this operation is normally performed at the factory. Thereafter, information can be read from the memory indefinitely.
RTC	(Real Time Clock) Peripheral circuitry on a computer motherboard which provides a nonvolatile time-of-day clock, an alarm, calendar, programmable interrupt, square wave generator, and a small amount of SRAM. In the NY1210, the RTC operates independently of the system PLL which generates the internal system clocks. The RTC is typically receives power from a small battery to retain the current time of day when the computer is powered down.
RS-232	A popular asynchronous bi-directional serial communication protocol. Among other things, the RS-232 standard defines the interface cabling and electrical characteristics, and the pin arrangement for cable connectors.
segment	A section or portion of addressable memory serving to hold code, data, stack, or other information allowing more efficient memory usage in a computer system. A segment is the portion of a real mode address which specifies the fixed base address to which the offset is applied.
serial port	A physical connection with a computer for the purpose of serial data exchange with a peripheral device. The port requires an I/O address, a dedicated IRQ line, and a name to identify the physical connection and establish serial communication between the computer and a connected hardware device. A serial port is often referred to as a COM port.
shadow memory	RAM in the address range 0xC000h through 0xFFFFFh used for shadowing. Shadowing is the process of copying BIOS extensions from ROM into DRAM for the purpose of faster CPU access to the extensions when the system requires frequent BIOS calls. Typically, system and video BIOS extensions are shadowed in DRAM to increase system performance.
SIMM	(Single In-Line Memory Module) A small, rectangular circuit board on which is mounted semiconductor memory ICs.
SODIMM	(Small Outline Dual Inline Memory Module) A new form factor for memory modules that is smaller and denser than SIMMs.

SRAM (Static Random Access Memory) A semiconductor RAM device in which the data remains permanently stored as long as power is applied, without the need for periodically rewriting the data into memory.

standoff A mechanical device, typically constructed of an electrically non-conductive material, used to fasten a circuit board to the bottom, top, or side of a protective enclosure.

symmetrically addressable SIMM A SIMM, the memory content of which is configured as two independent banks. Each 16-bit wide bank contains an equal number of rows and columns and is independently addressable by the CPU via twin row address strobe registers in the DRAM controller.

SYSCLK (ISAbus System Clock) The ~8.33MHz clock signal present on the ISAbus to which all bus transactions are synchronized.

system memory See *conventional memory*.

TB or TByte (Terabyte) Approximately one thousand billion (US) or one billion (Great Britain) bytes. 2^40 = 1,099,511,627,776 bytes exactly.

UED (User Editable Drive) A feature of the NY1210's Phoenix NuBIOS. When a "User" type hard disk drive setting shows in the IDE Adapter Sub-Menu the BIOS queries the hard disk drive for the purpose of retrieving disk geometry. If the hard disk drive is capable of providing this information, the BIOS uses it to automatically set up the drive for use with the system.

VESA (Video Electronics Standards Association) A group of hardware and software vendors that define specifications for hardware and software interfaces for a variety of devices.

VGA (Video Graphics Adapter) A popular PC graphics controller and display adapter standard developed by IBM. The standard specifies, among other things, the resolution capabilities of the display device. Display devices meeting the VGA standard must be capable of displaying a minimum resolution of 640 horizontal pixels by 480 vertical pixels with at least 16 screen colors.

wait state A period of one or more microprocessor clock pulses during which the CPU suspends processing while waiting for data to be transferred to or from the system data or address buses.

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